Advanced Micro Devices, Inc.

High-Speed Comparators

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Am685

Voltage Comparator

Distinctive Characteristics:

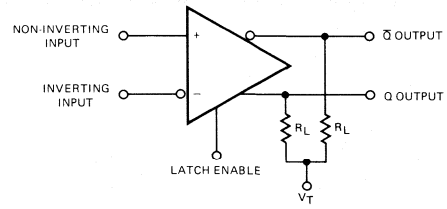
- **6.5ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE**
- 3.0ns Latch setup time
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in metal can and hermetic dual-in-line packages

FUNCTIONAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

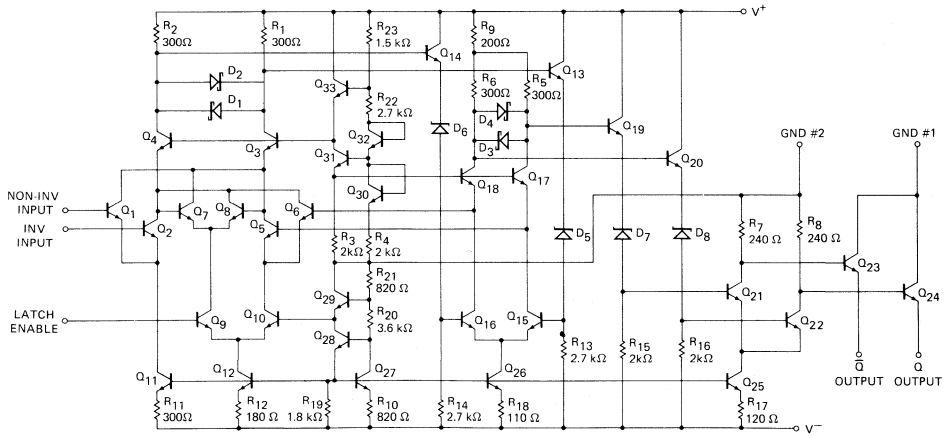
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0 V, or 200–2000Ω connected to −5.2 V.

CIRCUIT DIAGRAM



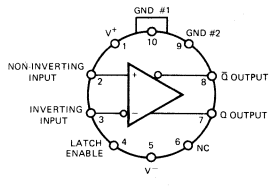
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am685	Metal Can	−30°C to +85°C	Am685HL
	DIP	−30°C to +85°C	Am685DL
Am685	Metal Can	−55°C to +125°C	Am685HM
	DIP	−55°C to +125°C	Am685DM
Am685	Dice	−30°C to +85°C	Am685XL
	Dice	−55°C to +125°C	Am685XM

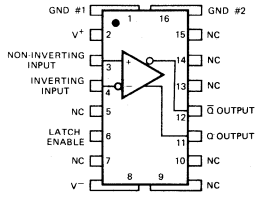
CONNECTION DIAGRAMS

Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 8 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	500 mW

Operating Temperature Range	
Am685-L	−30°C to +85°C
Am685-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd+}(E)	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}(E)	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
t_{pw}(E)	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

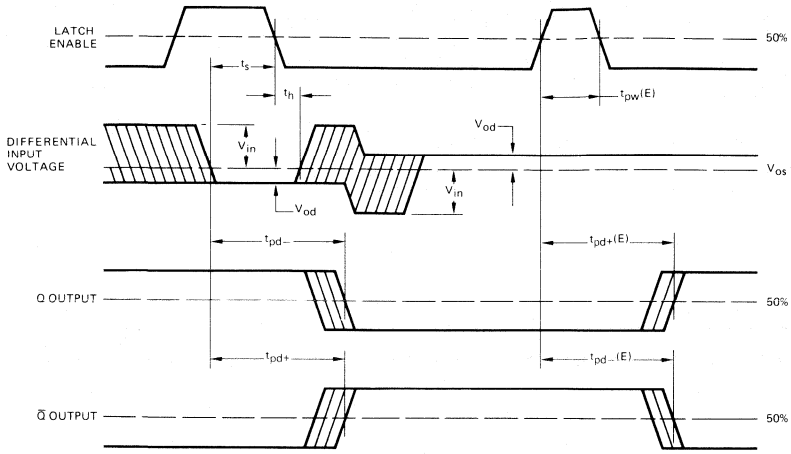
NOTES:

2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3: Unless otherwise specified $V^+ = 6.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

TIMING DIAGRAM



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

Figure 1

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** — The average of the two input currents.

R_{IN} **INPUT RESISTANCE** — The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** — The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I^+ **POSITIVE SUPPLY CURRENT** — The current required from the positive supply to operate the comparator.

I^- **NEGATIVE SUPPLY CURRENT** — The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** — The power dissipated by the comparator with both outputs terminated in 50Ω to -2.0V.

SWITCHING TERMS (refer to Fig. 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ **LATCH ENABLE TO OUTPUT HIGH DELAY** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ **LATCH ENABLE TO OUTPUT LOW DELAY** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **MINIMUM LATCH ENABLE PULSE WIDTH** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

OTHER SYMBOLS

T_A	Ambient temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{in}	Input pulse amplitude
V^+	Positive supply voltage	V_{od}	Input overdrive
V^-	Negative supply voltage	f	Frequency

MEASUREMENT OF PROPAGATION DELAY

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large- and small-signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100mV step with an overdrive of 5mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50% point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.

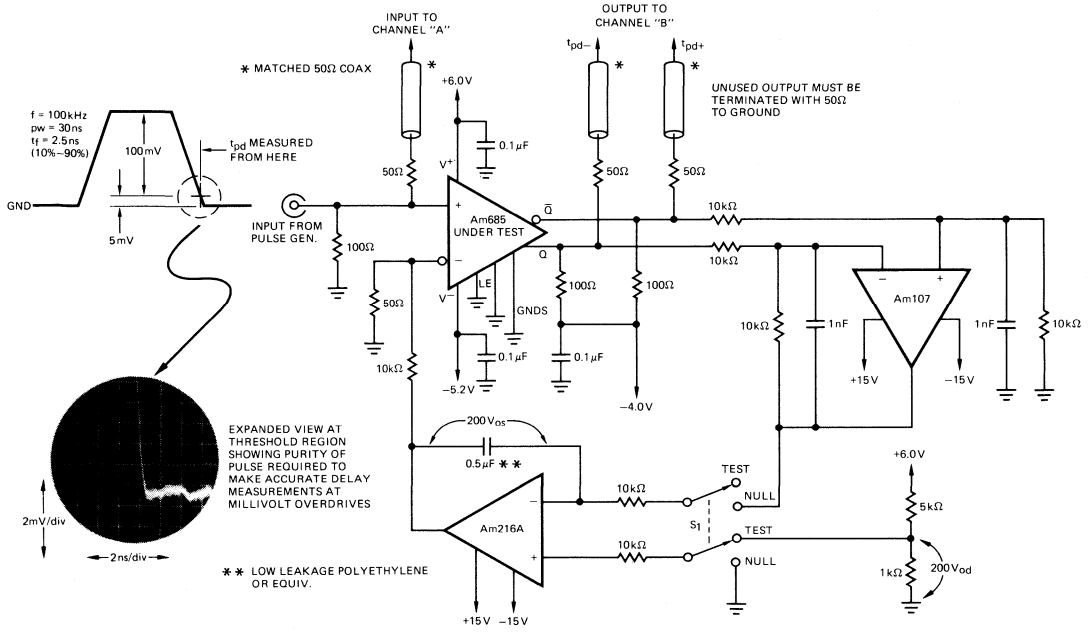


Figure 2

The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50Ω inputs of the sampling scope via equal lengths of 50Ω coaxial cable. For the conditions shown in the figure, t_{pd+} is measured at the $\overline{Q}$ output and t_{pd-} at the Q output. If it is desired to measure the opposite output polarities, the polarities of the input signal and overdrive must be reversed.

THERMAL CONSIDERATIONS

To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

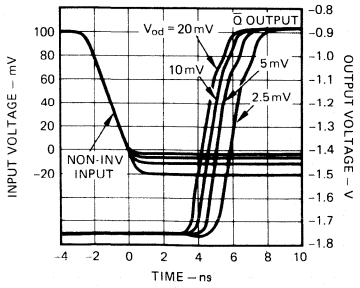
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60dB) at very high frequencies (100MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to -2.0V, but a Thevenin equivalent to V^- can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.

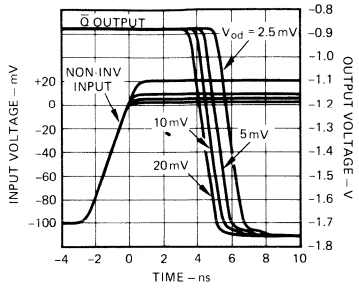
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

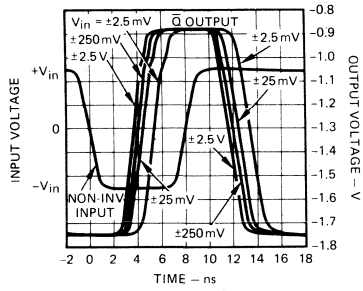
Response for Various Input Overdrives



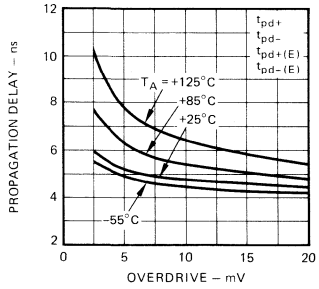
Response for Various Input Overdrives



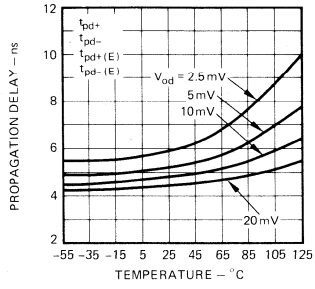
Response for Various Input Signal Levels



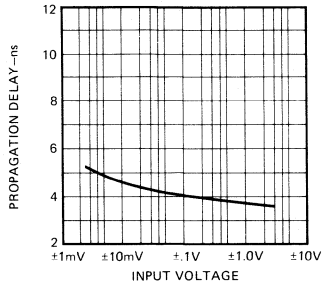
Propagation Delays as a Function of Input Overdrive



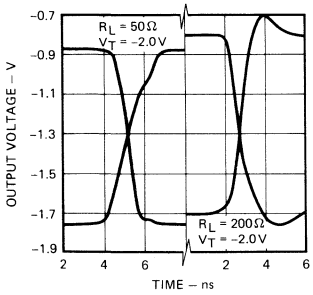
Propagation Delays as a Function of Temperature



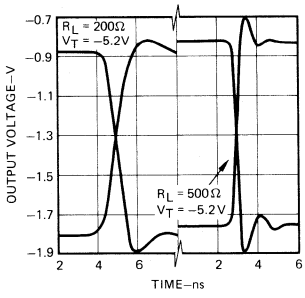
Propagation Delay as a Function of Input Signal Level



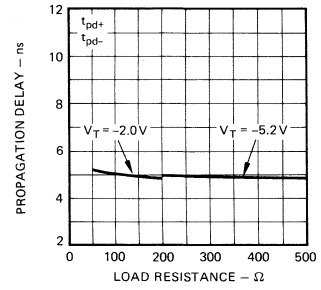
Response for Various Load Resistances



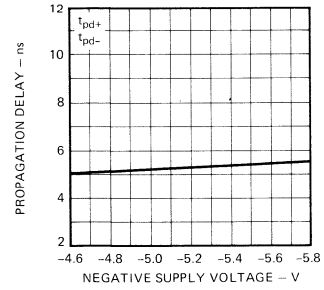
Response for Various Load Resistances



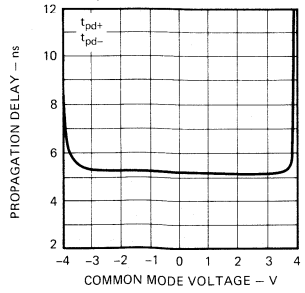
Propagation Delays as a Function of Load Resistance



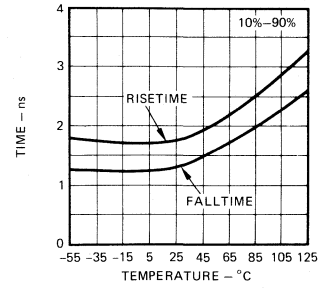
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



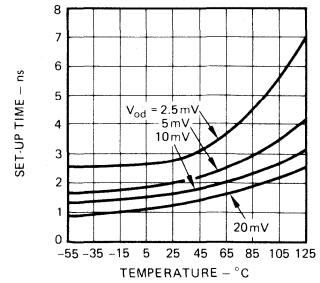
Output Rise and Fall Times as a Function of Temperature



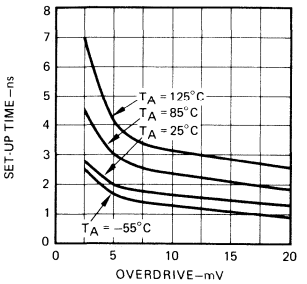
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

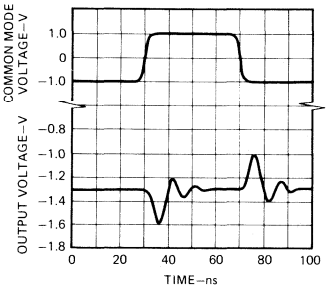
Set-up Time as a Function of Temperature



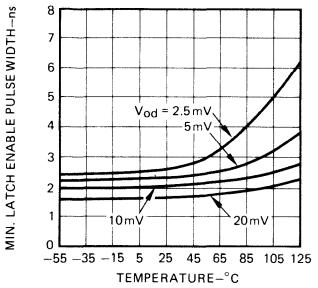
Set-up Time as a Function of Input Overdrive



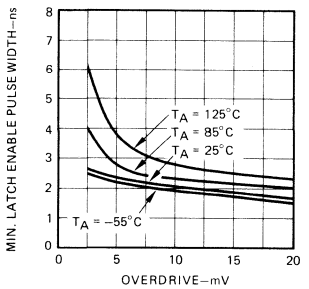
Common Mode Pulse Response



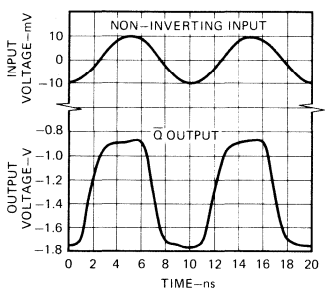
Min. Latch Enable Pulse Width as a Function of Temperature



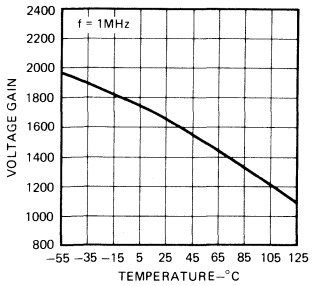
Min. Latch Enable Pulse Width as a Function of Input Overdrive



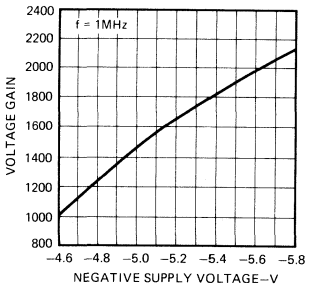
Response to 100MHz Sine Wave



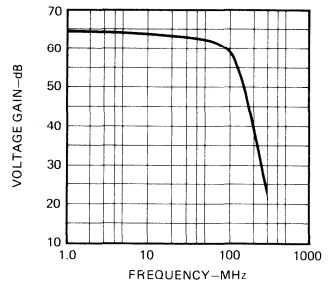
Voltage Gain as a Function of Temperature



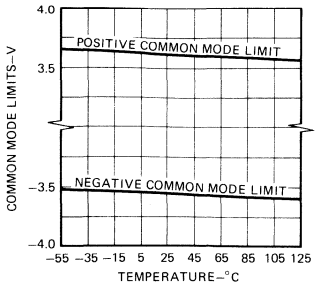
Voltage Gain as a Function of Negative Supply Voltage



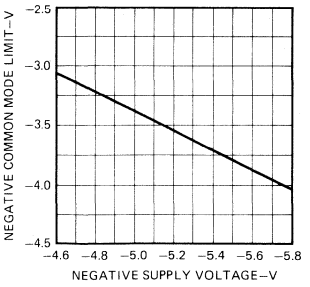
Voltage Gain as a Function of Frequency



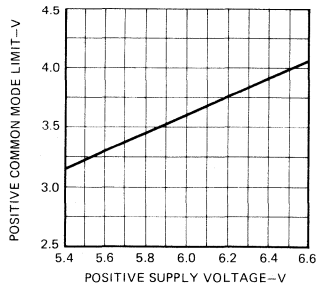
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



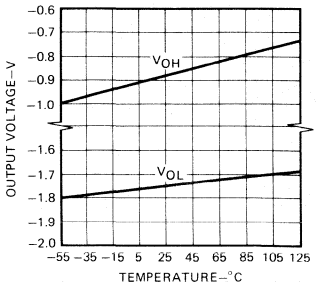
Positive Common Mode Limit as a Function of Positive Supply Voltage



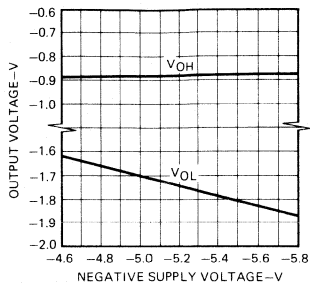
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

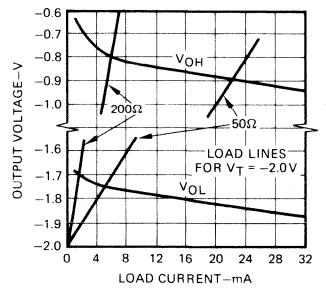
Output Levels as a Function of Temperature



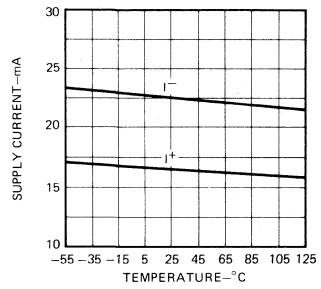
Output Levels As A Function Of Negative Supply Voltage



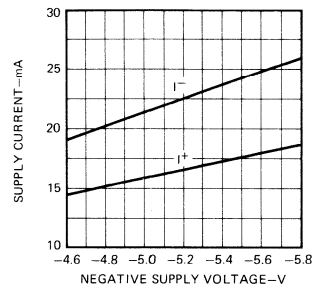
Output Levels As A Function Of DC Loading



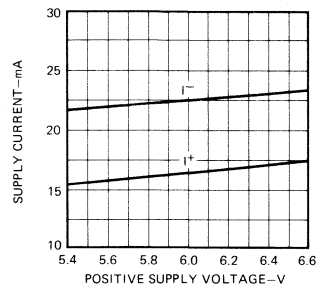
Supply Currents As A Function Of Temperature



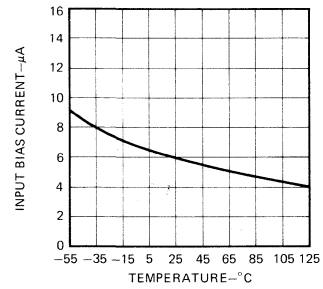
Supply Currents As A Function Of Negative Supply Voltage



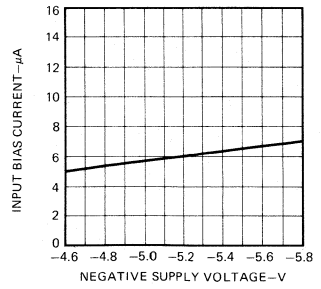
Supply Currents As A Function Of Positive Supply Voltage



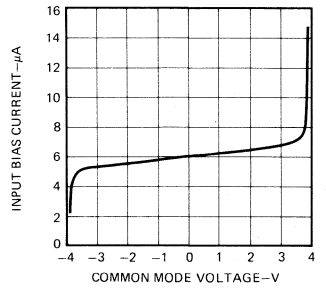
Input Bias Current As A Function Of Temperature



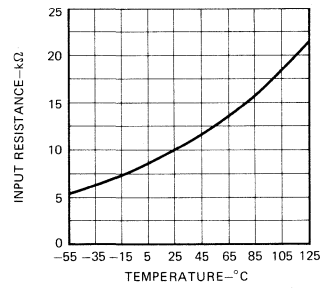
Input Bias Current As A Function Of Negative Supply Voltage



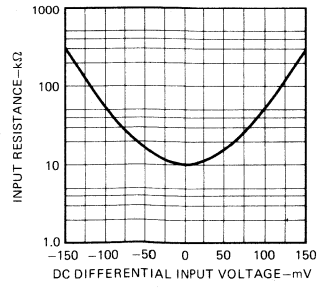
Input Bias Current As A Function Of Common Mode Voltage



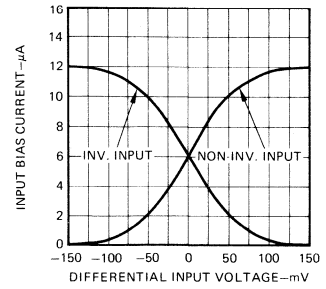
Input Resistance As A Function Of Temperature



Input Resistance As A Function Of DC Differential Input Voltage

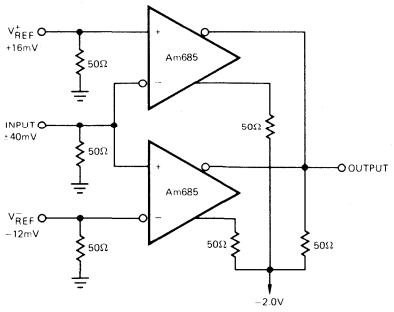


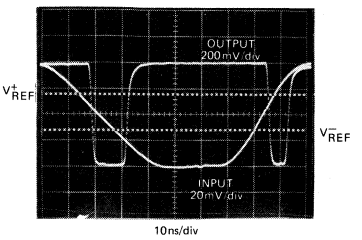
Input Current As A Function Of Differential Input Voltage



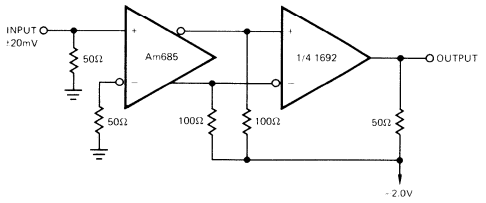
TYPICAL APPLICATIONS
(T_A = 25°C)

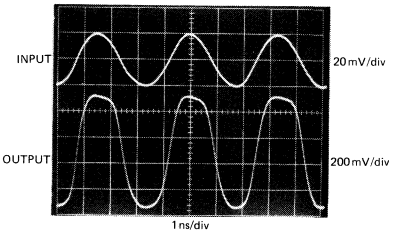
High-Speed Window Detector



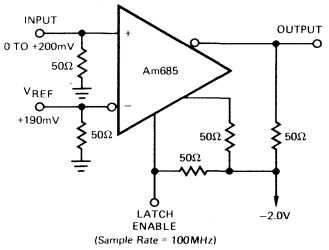


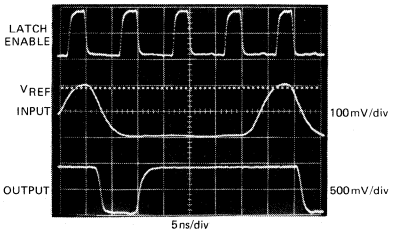
300MHz Line Receiver





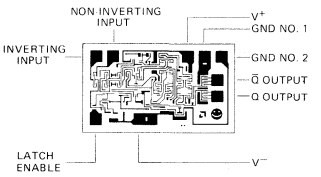
High-Speed Sampling





Metallization and Pad Layout

32 x 54 Mils



Am686
Voltage Comparator

Distinctive Characteristics

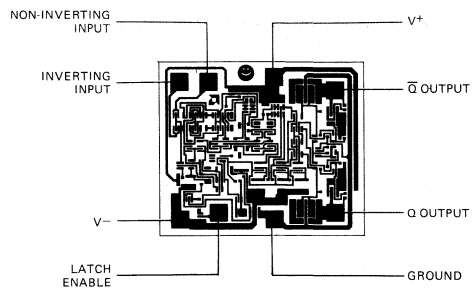
- 12ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary Schottky TTL outputs
- Fanout of 5
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can and hermetic dual-in-line packages.

FUNCTIONAL DESCRIPTION

The Am686 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with Schottky TTL. The output current capability is adequate for driving 5 standard Schottky inputs. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

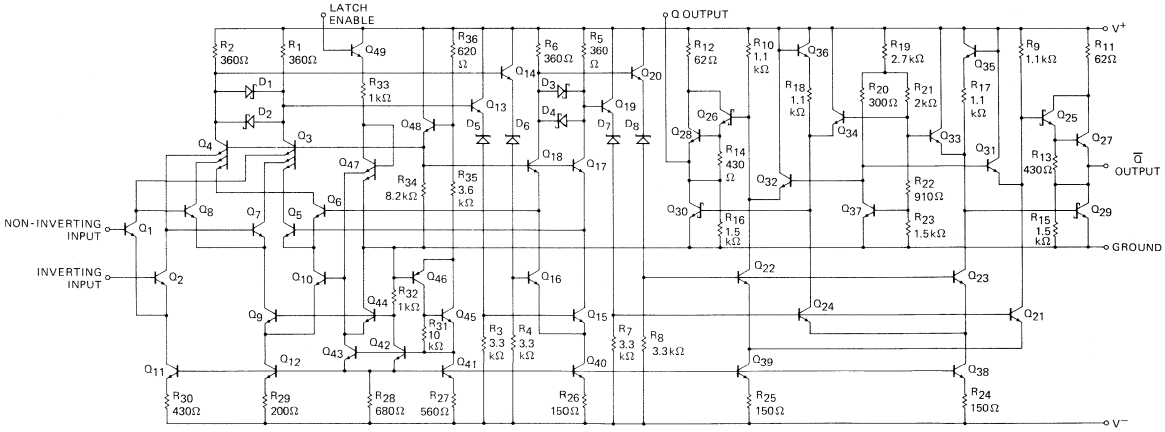
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is LOW, the comparator functions normally. When the Latch Enable is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable may be left open or connected to ground.

Metallization and Pad Layout



46 X 53 Mils

CIRCUIT DIAGRAM

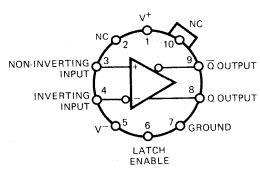


ORDERING INFORMATION

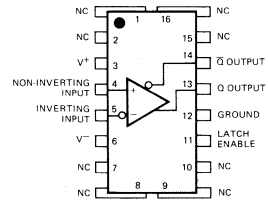
Part Number	Package Type	Temperature Range	Order Number
Am686	Metal Can	0°C to 70°C	Am686HC
	DIP	0°C to 70°C	Am686DC
Am686	Metal Can	−55°C to +125°C	Am686HM
	DIP	−55°C to +125°C	Am686DM
Am686	Dice	0°C to 70°C	Am686XC
	Dice	−55°C to +125°C	Am686XM

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 6 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7V
Negative Supply Voltage	−7V
Input Voltage	±4V
Differential Input Voltage	±6V
Power Dissipation (Note 2)	600mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C

Operating Temperature Range	
Am686-C	0°C to +70°C
Am686-M	−55°C to +125°C
Operating Supply Voltage Range	
Am686-C	V^+ = +5.0V ±5%, V^- = −6.0V ±5%
Am686-M	V^+ = +5.0V ±10%, V^- = −6.0V ±10%
Minimum Operating Voltage (V^+ to V^-)	9.7V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$	3.0 3.5	2.0 3.0	mV MAX. mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	10	10	µV/°C MAX.
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_A$ (max.) $T_A = T_A$ (min.)	1.0 1.3	1.0 1.6	µA MAX. µA MAX.
I_B	Input Bias Current	$25°C \leq T_A \leq T_A$ (max.) $T_A = T_A$ (min.)	10 13	10 16	µA MAX. µA MAX.
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	V MIN.
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3V \leq V_{CM} \leq +2.7V$	80	80	dB MIN.
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$	70	70	dB MIN.
V_{OH}	Output HIGH voltage	$I_L = -1.0mA$, $V_S = V_S$ (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	$I_L = 10mA$, $V_S = V_S$ (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

Switching Characteristics (V^+ = +5.0V, V^- = −6.0V, V_{in} = 100mV, V_{od} = 5.0mV, C_L = 15pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) $\leq T_A \leq 25°C$ $T_A = T_A$ (max.)	12 15	12 15	ns MAX. ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) $\leq T_A \leq 25°C$ $T_A = T_A$ (max.)	12 15	12 15	ns MAX. ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	$T_A = 25°C$	2.0	2.0	ns MAX.

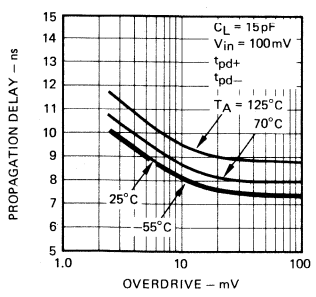
Notes: 2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.

3. Unless otherwise specified, V^+ = +5.0V, V^- = −6.0V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.

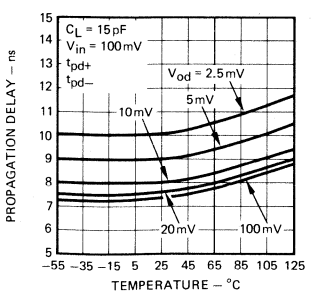
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

PERFORMANCE CURVES

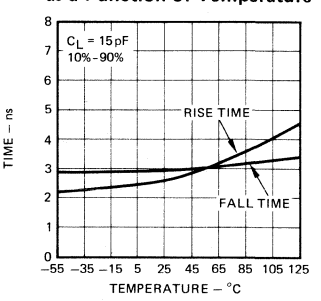
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



Am687·Am687A

Dual Voltage Comparators

Distinctive Characteristics

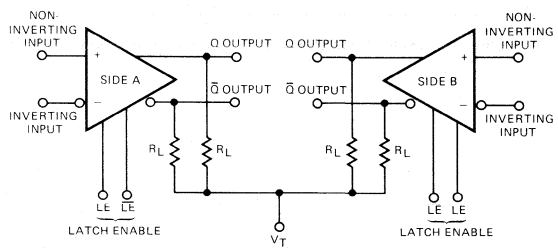
- 8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in the hermetic dual-in-line package.

FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

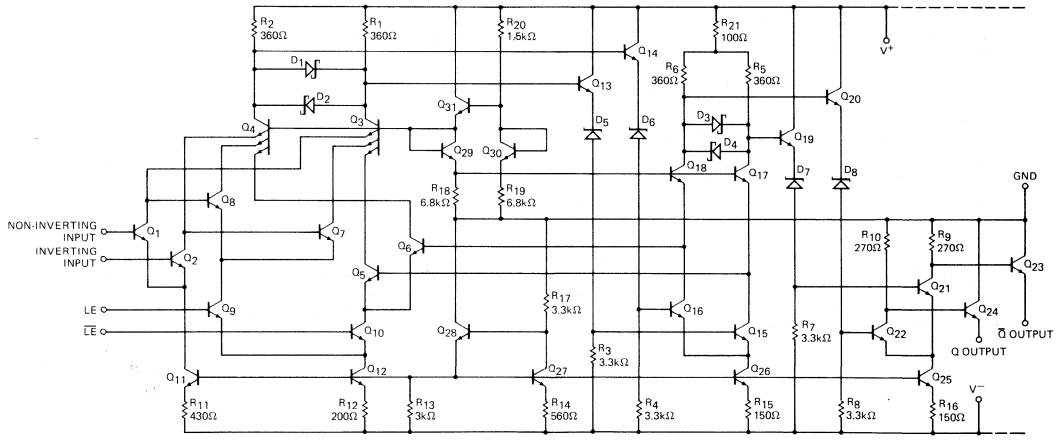
The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 6V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and $\overline{LE}$ is LOW, the comparator functions normally. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V, or 200–2000Ω connected to −5.2V.

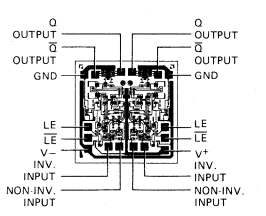
CIRCUIT DIAGRAM (Each Comparator)



ORDERING INFORMATION

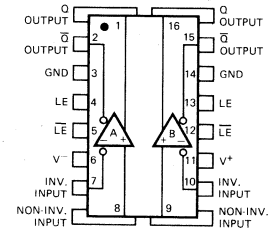
Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	−30°C to +85°C	AM687ADL
Am687A	DIP	−55°C to +125°C	AM687ADM
Am687	DIP	−30°C to +85°C	AM687DL
Am687	DIP	−55°C to +125°C	AM687DM
Am687	Dice	−30°C to +85°C	AM687XL
Am687	Dice	−55°C to +125°C	AM687XM

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.056"

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	600 mW

Operating Temperature Range	
Am687-L, Am687A-L	−30°C to +85°C
Am687-M, Am687A-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L Am687-L Min.	Am687A-L Am687-L Max.	Am687A-M Am687-M Min.	Am687A-M Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−3.5	+3.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$25°C \leq T_A \leq T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

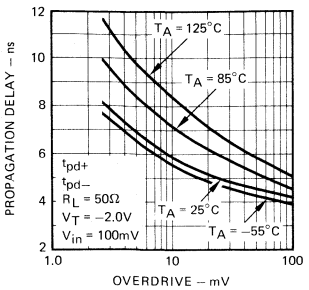
Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

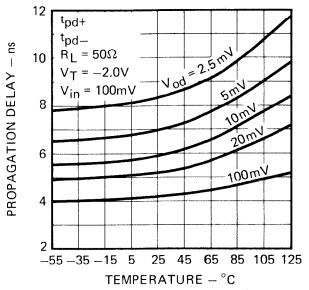
Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.
3. Unless otherwise specified $V^+ = +5.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

PERFORMANCE CURVES

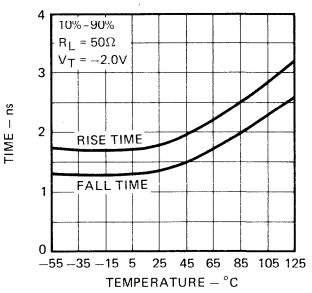
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



Am685/Am686/Am687 DESIGNING WITH HIGH SPEED COMPARATORS

By Leonard Brown

INTRODUCTION

The Am685, Am686 and Am687 are a family of high-speed sampling comparators capable of detecting low-level signals of the order of 5-10mV in 12-15ns over the temperature range $-55^{\circ}C \leqslant T_A \leqslant 125^{\circ}C$. The Am686 is fully TTL-compatible and complementary outputs are available generated from a true differential output stage assuring a maximum output skew of under 2ns at 25°C. The Am685 and Am687 are single and dual ECL-compatible versions, respectively, and have output skews of less than 1ns. A high-speed latch is incorporated in the input stage permitting input signals to be acquired in 4.0ns maximum for the ECL versions and 6.0ns for the TTL device.

Applications of the devices are not limited to high-speed designs as the combination of the excellent DC input characteristics, availability of true differential outputs and the latch function permit unique solutions for slower speed applications where the response time of the comparators can be considered negligible.

THE SAMPLING COMPARATOR

The sampling comparator may be visualized as a conventional voltage comparator with the provision that the outputs may be latched into the logic states determined by the **input signal conditions existing at the time of application of the latch signal.** This is achieved by incorporating the latch circuitry in the input stage of the device. The minimum latch enable pulse width is necessarily less than the propagation delay of the device and, therefore, the comparator can be unlatched for a fraction of its propagation delay (4.0ns for the Am685). The outputs will then change in accordance with the input conditions existing at the time of the latch signal. Note: It is impossible for the comparator to oscillate under these conditions.

If the latch function is not used, the device operates as a conventional voltage comparator.

BACK TO BASICS

Comparators are designed to have both high gain and large bandwidth. This creates instability problems or oscillations when the device outputs are in the transition region. The tendency of a device to oscillate is a function of the layout, (poor layout increasing the amount of feedback caused by parasitic capacitance) and the source impedance of the circuit employed (The higher the source impedance the less parasitic coupling is necessary to cause oscillation.) It is mandatory with comparators of the gain and bandwidth of the Am685, Am686 and Am687 to ensure that power supplies are well decoupled, lead lengths are kept as short as possible, and wherever possible (especially in the case of the Am686), a ground plane should be employed.

In addition to reducing the effects of stray capacitance, a ground plane substantially reduces the possibility of the output current spike coupling back to the inputs through the ground lead when the TTL output stages switch.

The minimum slew rate at which the input signal must cross the threshold region to prevent oscillation, regardless of the particular layout parasitics, may be determined by applying a DC voltage to the input until the circuit just commences to oscillate and increasing this voltage until the oscillation ceases. The minimum necessary input slew rate is then given by $\Delta V/t_{pd}$ MIN, where ΔV is the input voltage required to prevent oscillation and t_{pd} MIN is the minimum propagation delay of the comparator.

The minimum slew rate will be found to be a function of source impedance and source impedance mismatch.

The curves of Figures 1 and 2 show the minimum slew rate for the Am686 as a function of source impedance and source impedance mismatch.

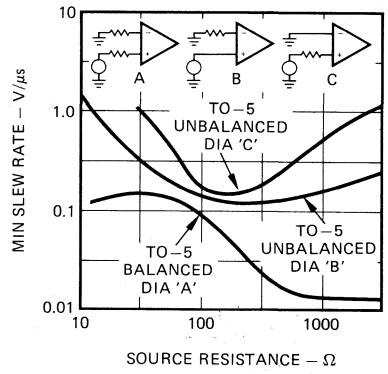


Figure 1. Minimum Slew Rate Versus Source Resistance (TO–5).

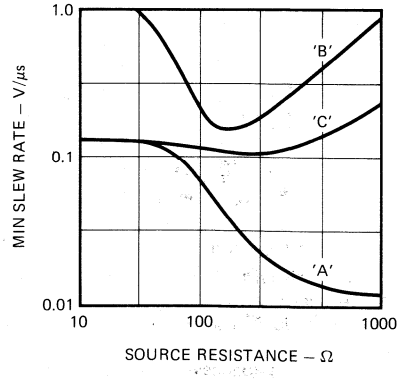


Figure 2. Minimum Slew Rate Versus Source Resistance (DIP).

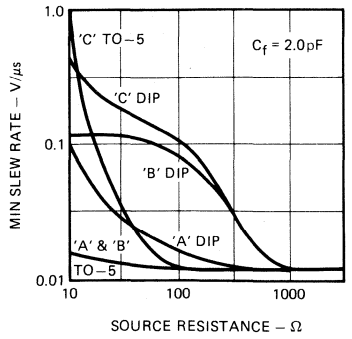


Figure 3. Minimum Slew Rate Versus Source Resistance (TO–5 & DIP).

It can be seen that unbalanced sources dramatically effect the minimum input slew rate required. Note that for optimum performance, the source impedance seen by the comparator should be both DC and AC balanced to reduce the differential feedback to a minimum.

The effect of an AC unbalanced source is seen especially on the Am686 as when the output switches, the output current spike is coupled back to the input. This can be eliminated by forcing the AC unbalance to result in positive feedback, which may be achieved by decoupling the inverting input or applying positive feedback via a 2-4pF capacitor from the Q output to the non-inverting input.

The curves of Figure 3 illustrate the improvement in minimum slew rate when a small amount of positive feedback is employed by virtue of a 2pF feedback capacitor.

OPTIMUM SOURCE CONDITIONS (C_f = 0pF)

With low source impedances ($< 50\Omega$), the majority of the feedback between the output and the input occurs internal to the device. As the source impedance is raised, external feedback increases through the parasitic feedback capacitance until, at high source impedances, the external feedback dominates. This explains the anomolous characteristics of the minimum slew rate curves and suggests that the optimum source resistance for the device is between 300 and 500Ω for unbalanced sources and is approximately 1000Ω for a balanced source.

OPTIMUM SOURCE CONDITIONS (C_f = 2pF)

With a source impedance of 100Ω, the minimum slew rate is 0.15V/μs for the DIP configuration and 0.02V/μs for the TO-5. For balanced sources the minimum slew rate is 0.03V/μs for $R_S \geq 100\Omega$ and for a source impedance between 1kΩ and 3kΩ, the minimum slew rate is <0.02V/μs regardless of impedance, DC imbalance or package type.

The use of the feedback capacitor is recommended when:

1. The input slew rate is within a factor of 2 greater than the minimum theoretical slew rate.
2. System constraints do not permit optimisation of layout and lead lengths.
3. Unbalanced source impedances are used (it is not always possible to provide input conditions which are both DC and AC balanced).

A FAMILY AFFAIR

It must be stressed that the concepts discussed concerning source imbalance and minimum input slew rate apply to all devices in the family. The Am686 was highlighted as it is more sensitive to layout constraints and parasitic feedback because of its significantly higher voltage gain.

Similarly all of the applications which follow may be implemented with any device in the series provided due caution is exercised with regard to the different output logic levels.

THE RELAXATION OSCILLATOR

The principal problems in the design of a classical relaxation oscillator are:

1. The variation in potential to which the energy storage device (normally a capacitor) is charged.
2. The variation in the threshold level at which the capacitor is to be discharged.
3. The variation inherent in the sensor element (normally a comparator) in detecting equivalence between the threshold level and the capacitor's instantaneous potential.

The variations are all functions of both time and temperature and are the primary causes of frequency drift, symmetry error, and jitter.

By taking advantage of two unique properties of the Am686, a relaxation oscillator may be designed to eliminate the first two problems and reduce the third to a second-order effect for oscillation frequencies from 1MHz to 30MHz.

The true differential output stage of the comparator ensures that the Q and $\overline{Q}$ outputs change within 1-2ns of each other. This feature ensures that the outputs can never be in the same logic state instantaneously, either HIGH or LOW, and that the only time they are equal in voltage is when traversing the logic uncertainty levels. This property permits the design of a threshold setting circuit that varies in accordance with the charging voltage applied to the timing capacitor. Therefore, any change in charging potential is automatically compensated by a corresponding change in threshold level.

Second, the combination of the short propagation delay 7-10ns, the minimum difference in propagation delay between outputs and the stability of these delays with temperature assures square wave symmetry of better than 1% @ 1MHz and 5% @ 25MHz and a frequency stability of 1% @ 10MHz and 4% @ 25MHz.

The above statements are true from device to device and over the operating temperature range of –55°C to +125°C. Over the industrial temperature range, a factor of two improvement should be obtained.

CIRCUIT THEORY (Fig. 4)

Assuming the circuit is in an oscillating mode, the voltage appearing at the non-inverting terminal will alternate between V_X and V_Y where:

$$V_X = \frac{R_1}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL} \quad \text{and}$$

$$V_Y = \frac{R_2}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL}$$

When $V_{+IN} = V_X$, the timing capacitor C will be charging towards V_{OH}, and when $V_{+IN} = V_Y$, the timing capacitor will be discharging towards V_{OL}.

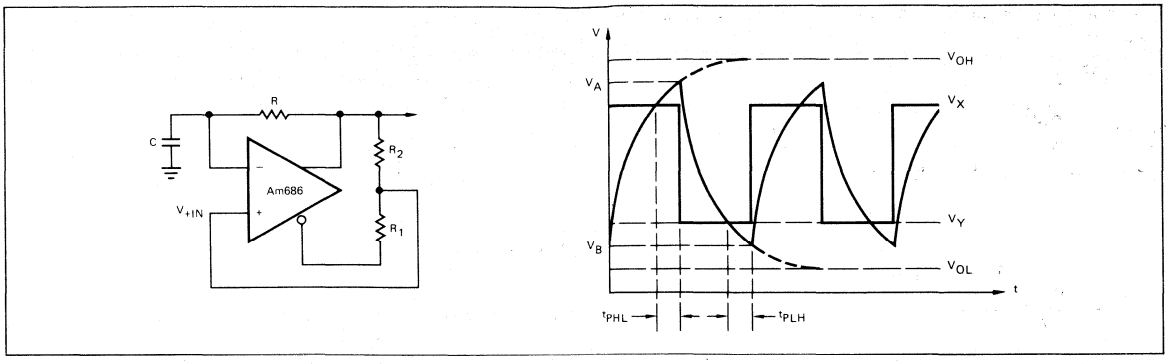


Figure 4. Circuit Design.

After the voltage on the capacitor equals the voltage on the non-inverting input, a finite time will elapse before the output of the circuit changes, during which time (the propagation delay of the Am686) the capacitor will continue to charge towards V_{OH}, or discharge towards V_{OL}.

Therefore, the capacitor will charge to a voltage

$$V_A = V_{OH} - e^{-t_{PHL}/CR} \cdot (V_{OH} - V_X)$$

and discharge to a voltage

$$V_B = V_{OL} + e^{-t_{PLH}/CR} \cdot (V_Y - V_{OL})$$

where t_{PHL} and t_{PLH} = propagation delay of the Am686 from the inputs to the output changing from HIGH – LOW and LOW – HIGH respectively.

The time to charge from V_B to V_A which is the positive half cycle is given by:

$$t^+ = CR\ 1n\ \frac{V_{OH} - V_B}{V_{OH} - V_A}$$

substituting for V_A and V_B

$$\mathbf{t^+ = CR\ 1n\ [(\frac{R_1}{R_2} + 1)\ e^{tPHL/CR} - 1]}$$

Similarily the negative half cycle is given by:

$$t^- = CR\ 1n\ \frac{V_A - V_{OL}}{V_B - V_{OL}}$$

$$\mathbf{t^- = CR\ 1n[(\frac{R_1}{R_2} + 1)\ e^{tPLH/CR} - 1]}$$

Note: The only assumptions are:

1. $(V_{OH} - V_{OL})$ of the Q output = $(V_{OH} - V_{OL})$ of the $\overline{Q}$ output.
2. Offset voltage and offset current errors are negligible.
3. $e^{t_{PLH}/CR} \times e^{-t_{PHL}/CR} = 1$

The only factor affecting pulse width variation is, therefore, t_{PHL} and t_{PLH}. As $t_{PHL} > t_{PLH}$ by 1-2ns, it is therefore anticipated that t^+ will be marginally greater than t^-.

MINIMUM OPERATING FREQUENCY

For the Am686, it is specified that the minimum slew rate at the input to insure that the device will not oscillate in the transition region is 1V/μs. This will determine the minimum operating frequency of the circuit.

The rate of change of voltage on the timing node is given by:

$$\rho = \frac{\partial v}{\partial t} = \frac{Vo}{CR} \times e^{-t/CR}$$

In the circuit,

a) $Vo = V_{OH} - V_B$ (assuming positive ramp)

and

b) $t = CR\ 1n\ [(\frac{R_1}{R_2} + 1)\ e^{t_{PHL}/CR} - 1]$

As the slew rate is only critical in determining the lowest operating frequency, it may be assumed that $e^{t_{PHL}/CR} = 1$ $(CR >>> t_{PHL})$; therefore, $Vo = V_{OH} - V_B \approx V_{OH} - V_Y$

$$Vo = (V_{OH} - V_{OL})\ \frac{R_1}{R_1 + R_2} \qquad \text{and, } t = CR\ 1n\ \frac{R_1}{R_2}$$

$$\therefore \rho = \frac{\partial v}{\partial t} = \frac{(V_{OH} - V_{OL})}{CR} \times \frac{R_1}{R_1 + R_2} \times \frac{R_2}{R_1}$$

$$= \frac{\Delta V}{CR} \times \frac{R_2}{R_1 + R_2}$$

where, $\Delta V = (V_{OH} - V_{OL})$

The minimum operating frequency

$$f_{MIN} = \frac{1}{2\ CR\ 1n\ \frac{R_1}{R_2}}$$

substituting

$$CR = \frac{\Delta V}{\rho}\ \frac{R_2}{R_1 + R_2} \qquad f_{MIN} = \frac{\rho}{2\Delta V} \times \frac{(R_1/R_2 + 1)}{1n\ R_1/R_2}$$

The expression for minimum frequency indicates that an optimum ratio of R_1/R_2 exists that is independent of any particular RC time constant which may have been chosen.

The ratio may be determined by differentiating f_{MIN} with respect to R_1/R_2.

$$\frac{\partial f_{MIN}}{\partial \frac{R_1}{R_2}} = \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - \left(\frac{R_1}{R_2}+1\right)/\frac{R_1}{R_2}}{\left(1n\frac{R_1}{R_2}\right)^2}$$

$$= \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1}}{\left(1n\frac{R_1}{R_2}\right)^2}$$

Setting $\frac{\partial F}{\partial \frac{R_1}{R_2}} = 0$

$$1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1} = 0$$

$$\frac{R_1}{R_2} = \frac{1}{1n\frac{R_1}{R_2} - 1}$$

$$\therefore \frac{R_1}{R_2} = 3.59112$$

Therefore, the lowest frequency the oscillator will perform consistent with the 1V/μs constraint is:

$$f_{MIN} = \frac{1 \times 4.6}{2 \times 3.5\ 1n\ 3.6} = .513MHz$$

D.C. OFFSET ERRORS

The presence of DC errors resulting from the bias and offset currents and offset voltage of the Am686 will cause the V_Y and V_X thresholds to be both shifted either positive or negative by an equal amount δV where δV is the sum of all such errors.

The magnitude of these effects may be calculated as follows:

When the capacitor is discharging –

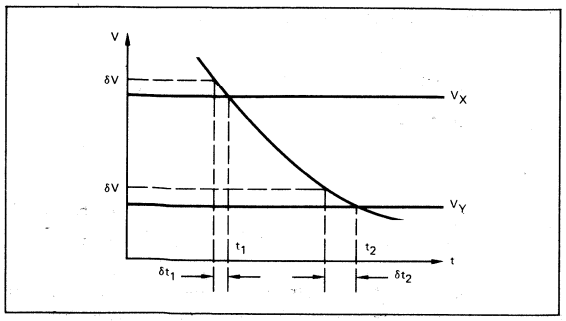


Figure 5.

$$V_{(t)} = V_o e^{-t/CR}$$

$$\frac{dv}{dt} = -\frac{1}{CR} Vo e^{-t/CR} = -\frac{1}{CR} V_{(t)}$$

$$\delta t_1 = -\frac{\delta V}{V_{(t_1)}} CR$$

$$\delta t_2 = \frac{-\delta V CR}{V_{(t_2)}}$$

Δt^- Negative Pulse Width Change =

$$\delta t_2 - \delta t_1 = \delta VCR \frac{V_{(t_2)} - V_{(t_1)}}{V_{(t_1)}\ V_{(t_2)}}$$

As $V_X = V_{t_1}, V_Y = V_{t_2}$

$$\Delta t^- = \frac{\delta VCR\ (V_Y - V_X)}{V_X V_Y}$$

Similarly for the positive pulse

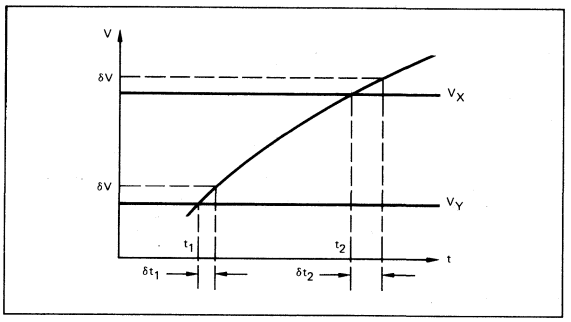


Figure 6.

$$V_{(t)} = Vo\ (1 - e^{-t/CR})$$

Whence, $dv/dt = \frac{1}{CR}(Vo - V_{(t)})$

$$\therefore \delta t_1 = \frac{\delta VCR}{Vo - V_{t_1}}$$

$$\delta t_2 = \frac{\delta VCR}{Vo - V_{t_2}}$$

Positive Pulse Width Change $\Delta t^+ = \delta t_2 - \delta t_1$

$$= \delta VCR \frac{1}{Vo - V_{(t_2)}} - \frac{1}{Vo - V_{(t_1)}}$$

In the circuit $V_{t_2} = V_X, V_{t_1} = V_Y, Vo - V_X = V_Y$

$$\Delta t^+ = \delta VCR \left(\frac{1}{V_Y} - \frac{1}{V_X}\right) = \delta VCR \frac{V_X - V_Y}{V_X V_Y} = -\Delta t^-$$

∴ Offset errors do not affect the frequency of oscillation, only the symmetry of the waveshape.

SYMMETRY ERROR

$$\text{Symmetry } S = \frac{\Delta t^+ - \Delta t^-}{2T} \times 100\% \text{ where } T = CR\ 1n\ \frac{V_Y}{V_X}$$

$$S = \frac{2\Delta t^+}{2T} \times 100\%$$

$$= \frac{\delta VCR\ (V_X - V_Y)}{V_X V_Y} \times \frac{1}{CR\ 1n\ V_Y/V_X}$$

Symmetry is worse for maximum value of $V_X - V_Y$. Maximum value of $V_X - V_Y$ occurs when R_1 and R_2 are arranged for minimum operating frequency, i.e., $R_1/R_2 = 3.6$

Substituing $\delta V = 5mV$

$$V_X/V_Y = 3.6$$

$$V_X V_Y = \frac{1}{4.6} V_{OH} \times \frac{3.6}{4.6} V_{OH}$$

$$V_{OH} = 3.5V \text{ and neglecting } V_{OL}$$

Symmetry is $< 0.38\%$

Note: 1. For any given ratio of $R_1 : R_2$ (i.e., V_X and V_Y), offset voltage Symmetry error is independent of frequency.

2. Symmetry improves to .33% @ $R_1 : R_2 = 2.5$

EXTENDING LOW FREQUENCY PERFORMANCE

If it is necessary to extend the lower limit of the oscillation frequency, a small amount of positive feedback may be introduced by connecting a 2-4pF capacitor between the Q output and the non-inverting input. This will decrease the minimum input slew rate required and enable oscillation frequencies of 1kHz to be achieved without spurious oscillations occuring on the rising or falling edges of the waveform. At frequencies below 1MHz, it is not necessary to take into account any potential frequency shift this additional feedback introduces. (Above 1MHz, it is not necessary to use this additional feedback.)

PERFORMANCE CHARACTERISTICS:

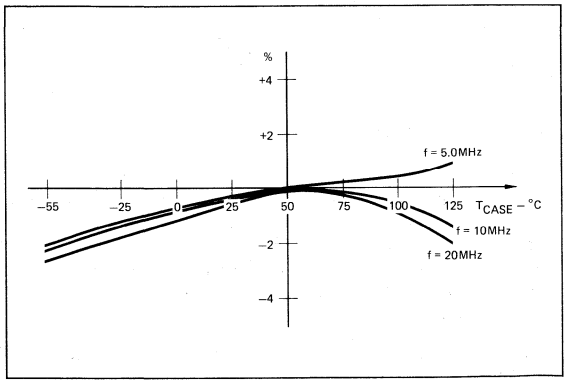


Figure 7. Percentage Change in Frequency Versus Case Temperature.

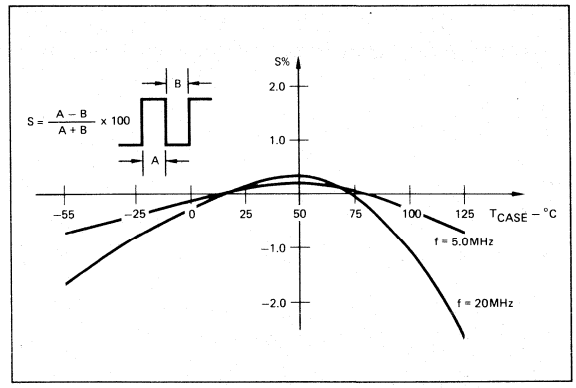


Figure 8. Change in Symmetry Versus Case Temperature.

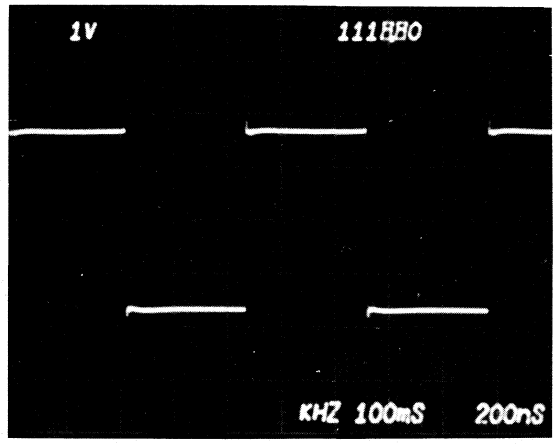


Figure 9. Output Waveform at 1.0MHz.

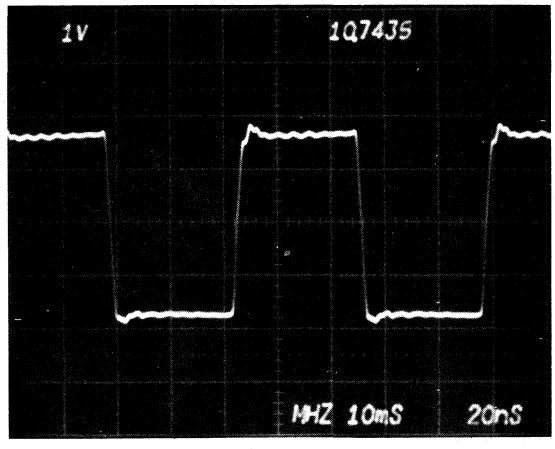


Figure 10. Output Waveform at 10MHz.

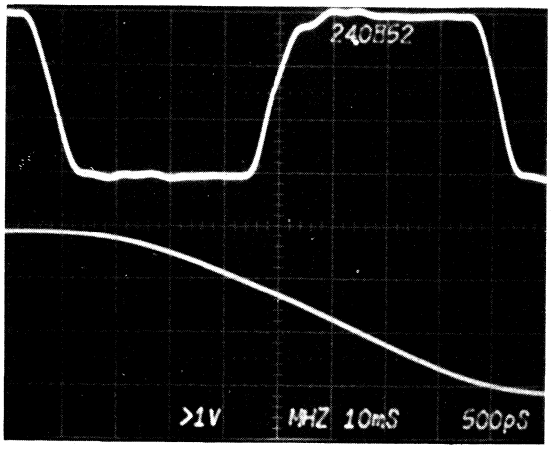


Figure 11. Output Waveform at 24MHz and Expanded Falling Edge Exhibiting <50ps Jitter.

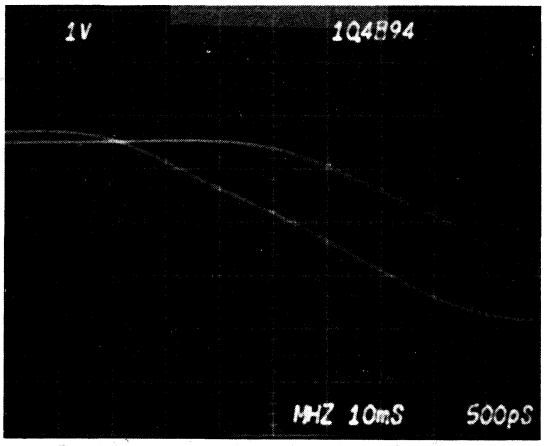


Figure 12. Change in Pulse Width and Jitter from 25°C to 125°C, f = 10MHz.

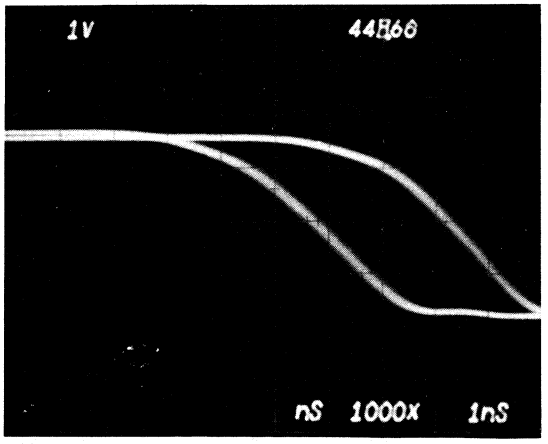


Figure 13. Expanded Fall Time Showing Change in Pulse Width from 25°C to 125°C, f = 1.0MHz, (Jitter ~ 300ps).

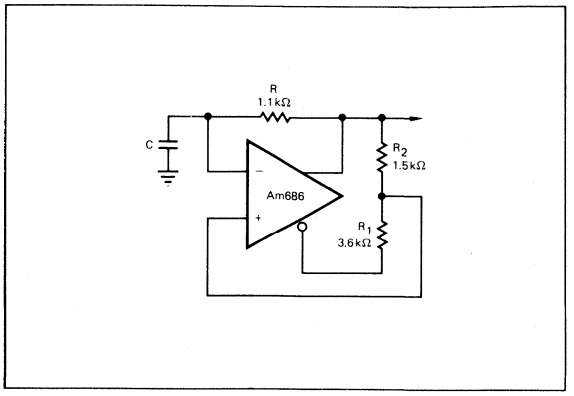


Figure 14. Circuit and Component Values used in Obtaining Performance Characteristics.

LOW LEVEL PULSE DETECTOR

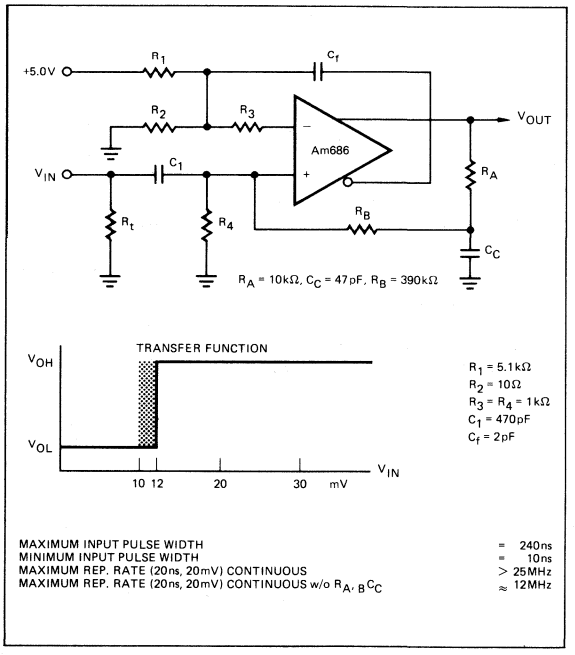


Figure 15.

CIRCUIT OPERATION

The input resistance is essentially determined by R_4 which was chosen to be 1kΩ on the basis that most sources would not be unduly loaded at this value and consequentially higher values would make the circuit excessively prone to oscillation. To minimize bias current errors, the inverting input is connected to the 10mV reference source (R_1 and R_2) through an equal-valued resistor (R_3).

Positive feedback is provided by C_f which provides a 50-60mV, 3-4ns pulse, significantly improving the switching time and narrowing the uncertainty region for pulses just in excess of the 10mV threshold.

Capacitor C_1 provides A-C coupling and thus isolates the circuit from slowly varying signals which may be superimposed on the signal to be detected. Such is the case for a detector sensing the output from a fibreoptic cable receiver. The A-C coupling imposes additional constraints; namely, the repetition rate and duty cycle of the input signal.

The signal which is seen by the non-inverting terminal and then compared to the reference is not simply the peak value of the input pulse but the peak value less the average D.C. value of the input signal.

Assuming a 20mV input pulse, 20ns wide and repeated every 20ns, the signal seen across R_4 will be as follows:

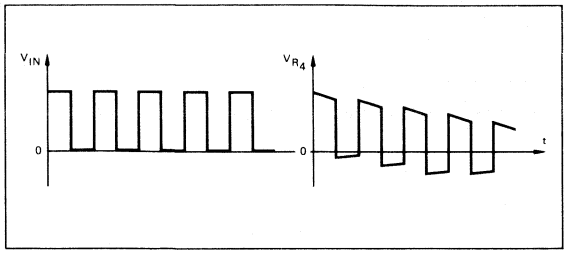


Figure 16.

By the ninth pulse, the peak signal will be 15.2mV dropping to 14.6mV by the end of the pulse; thus, after a pulse train of ~10 pulses, the detector will not detect the incoming signal.

Additionally, consider the case of a 20ns pulse repeated every 60 nanoseconds.

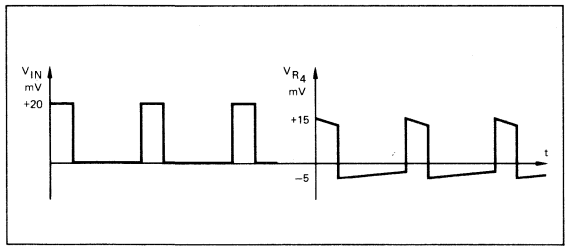


Figure 17.

The peak signal at the input will now be only 15mV; therefore, the maximum repetition rate consistent with providing a 5.0mV overdrive is 1/80ns or 12.5MHz.

Therefore, the circuit will only successfully detect 20mV, 20ns signals if: a) the pulse train is ⩽ 10 pulses or b) the repetition rate ⩽ 12MHz.

To compensate for these problems, a DC feedback signal is generated by R_A, R_B and C_C, which adjusts the reference level accordingly.

R_A and C_C form a low-pass filter that gives a maximum DC level of 1.7 volts at a 1:1 duty cycle. At this duty cycle, it is required to reduce the reference level by 5mV to maintain adequate overdrive. R_B and R_4 form an attenuator and the DC voltage level returned to the non-inverting input = 1.7V x $R_4/(R_4 + R_B)$ = 4.3mV. Using this network permits the circuit to work up to 25MHz, or better than a 1 : 1 duty cycle and removes the limitation imposed by the input A-C coupling.

Note: The response time of the feedback path must be the same as the input network; i.e., $R_AC_C = R_4C_1$ in order for the feedback to follow rapid changes in repetition rate or duty cycle.

PRECISION MONOSTABLE

Commercially available one-shots encounter problems in the generation of narrow (< 100ns) pulses. Namely, there is a significant delay between the input pulse and the output pulse of the order of 20ns and the resultant output pulse width is highly temperature dependent due to the variation in internal delays with temperature. Second, the input pulse must be of the logic level for the type of logic employed in the design — TTL, DTL, RTL, etc. Thus, the circuits are incapable of responding to low-level input signals in the millivolt range.

The Am685 series of sampling comparators can be employed in the design of a custom one-shot to overcome both of these problems.

Figure 18 shows the design of a monostable employing the Am686 to generate precision output pulses in the 20-100ns range and the values shown are for a 50ns pulse width.

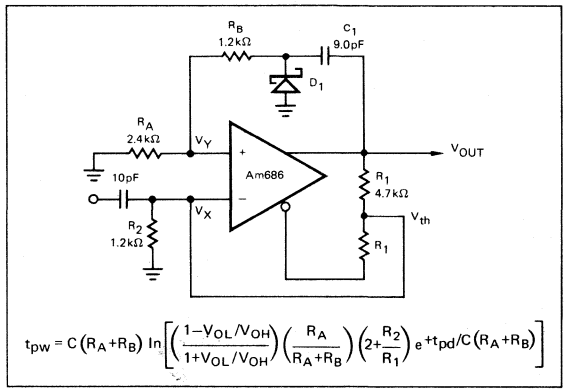


Figure 18.

The timing diagram illustrates the circuit operation.

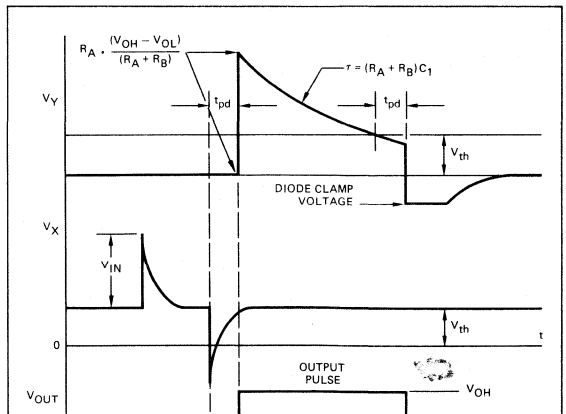


Figure 19.

The circuit triggers on the negative-going edge of the input pulse and the Q output switches high. The output signal is attenuated by R_A and R_B to keep the coupled pulse inside the common mode limits of the device. The output remains high until the voltage on the non-inverting input reaches the threshold set by R_1 and R_2. In order that the pulse width be independent of the input pulse amplitude, it is important to make the input time constant small compared to the desired output pulse width.

A unique feature of the circuit is the use of the differential outputs of the device to set the threshold, V_{th} thus providing temperature compensation and a reduction in pulse width variation from device to device.

Diode D_1 shortens the recovery time of the timing capacitor and permits retriggering 30ns after the end of the pulse with less than a 5% change in pulse width.

Complete isolation of the input signal and the timing network may be achieved by employing the latch function as shown below:

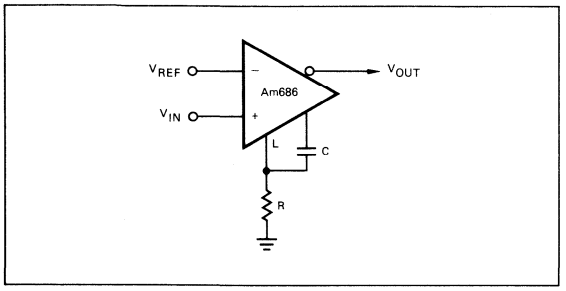


Figure 20.

When the input signal exceed V_{REF}, the output will switch and latch the comparator in the high state. When timing capacitor charges to the latch threshold, the latch will become disabled and the output will switch back to zero, providing the input is now below V_{REF}.

The advantages of this approach are:

1. No interaction between input signal and timing capacitor.
2. The input threshold set by V_{REF} is independent of the timing threshold.

Thus, the input threshold can be varied from millivolts to volts. A practical circuit is shown:

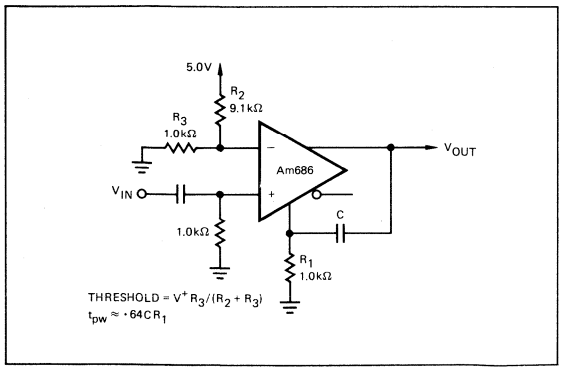


Figure 21.

The circuit is applicable for situations where accuracy of trigger threshold is important, a large variation in input signal level is expected or the input signal level is low. Timing accuracy (pulse width) is independent of the amplitude of the input pulse, but the output pulse width varies with temperature in accordance with the temperature dependence of the latch threshold (~ 3.0mV/°C for Am686).

APPLICATIONS REQUIRING INPUT HYSTERESIS

Comparators are frequently employed in systems where it is required that the transfer function contain a defined amount of hysteresis. Conventional comparators employing positive feedback can be used to generate hysteresis as shown below:

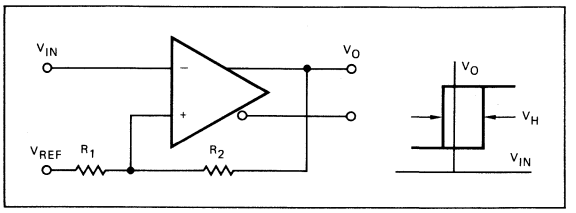


Figure 22.

Drawbacks of this technique include:

1. Response time of hysteresis loop ⩾ comparator propagation delay
2. Hysteresis varies with V_{OH} and VOL changes
3. Hysteresis is not centered about zero unless an additional reference is used.

By utilizing the latch function on the Am685, Am686 and Am687, hysteresis can be inserted in a manner to overcome these drawbacks; namely:

1. **Response time of hysteresis loop << propagation delay**
2. Hysteresis not affected by V_{OH} and V_{OL} changes
3. Hysteresis is symmetrical about zero.
4. **Full input differential capability maintained over complete common mode range.**

The hysteresis is obtained by applying a slight bias to the latch inputs. The technique is illustrated in the test circuit shown for the Am687.

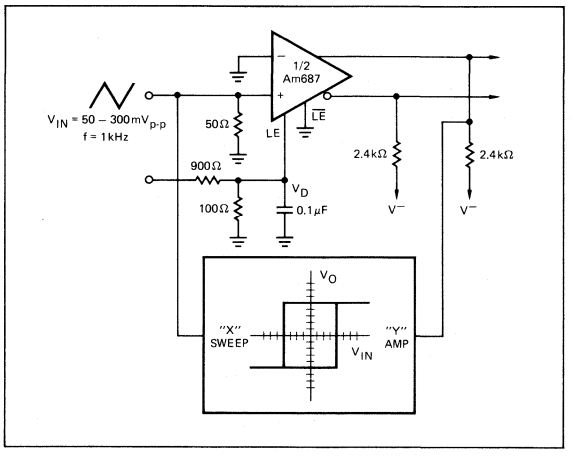


Figure 23.

The hysteresis is essentially symmetrical about zero and between ±5 and ±50mV of hysteresis can be generated before the relationship between the latch voltage and the thresholds become too sensitive.

The hysteresis is independent of changes in the positive supply voltage and the input common mode range and varies only with changes in temperature and negative supply voltage.

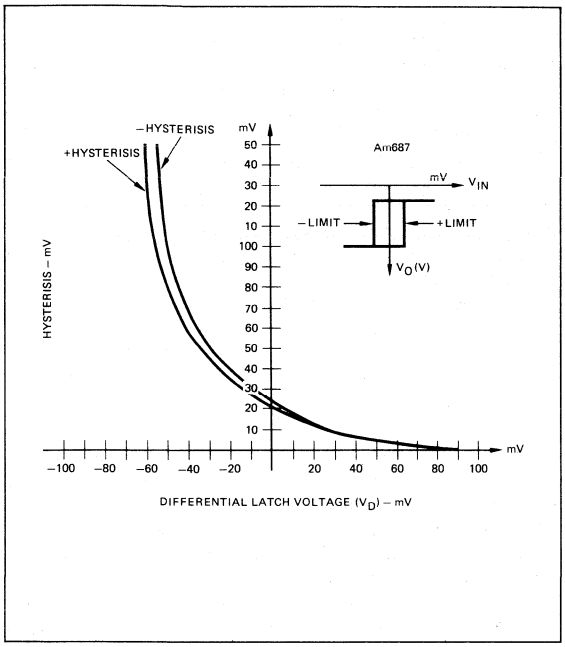


Figure 24. Input Hysteresis Versus Latch Voltage, T_A = 25°C.

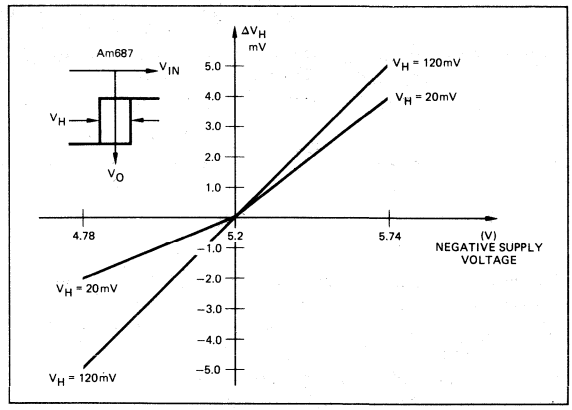


Figure 25. Change in Hysteresis Versus Change in Negative Supply Voltage.

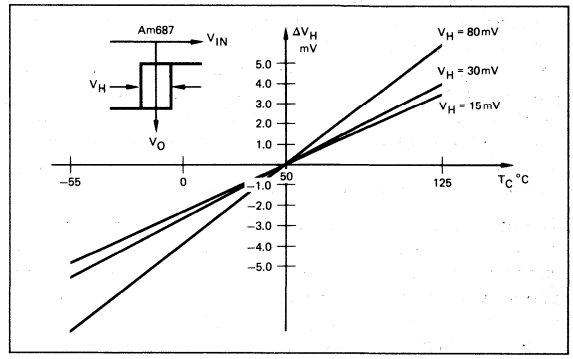


Figure 26. Change in Hysteresis Versus Case Temperature.

A NEW HIGH-SPEED COMPARATOR THE Am685

By Jim Giles and Alan Seales

INTRODUCTION

Modern electronic systems require more and more that operations be performed in a few nanoseconds so that the delay of the complete system, which may be very complex, be held to a minimum. There are abundant logic circuit elements available that meet this criterion: gold-doped TTL, Schottky TTL, and emitter-coupled logic (ECL), listed in descending order of propagation delay. Where it is necessary to interface from the analog world to the input of a logic system, or to detect very low-level logic signals in the presence of heavy noise, a high-speed precision comparator is needed. If such a comparator had a propagation delay less than 10ns, it could replace costly and complex circuitry that designers are now forced to use in very high-speed analog-to-digital converters, data acquisition systems, and optical isolators, as well as make possible many applications hitherto considered unfeasible. It could also be used as a sensitive line receiver or sense amplifier, in 100MHz sample and hold circuits, and in very high-frequency voltage-controlled oscillators.

The basic requirements for a high-speed precision comparator are few and well-defined: good resolution (high gain), high common-mode and differential voltage ranges, outputs compatible with standard logic levels, and, above all, very fast response to signal levels ranging from a few millivolts to several volts. The industry workhorse, the 710, has come close to meeting these requirements, and except for the most demanding applications, its 40ns propagation delay is adequate. A survey of presently available monolithic IC comparators (Table I) shows that there is really none that meets the requirements of very high-speed systems. The newer TTL-output circuits offer only marginal improvement over the 710 when measured under identical conditions of large input pulse and small overdrive, and the ECL-output comparator, although faster, has such poor resolution that it can be used only for large input signals. Advanced Micro Devices felt there was a need for a family of linear devices to fill the needs of very high-speed systems, with the first circuit being a precision comparator with less than 10ns delay.

Type No.	Logic Family	Propagation Delay	Resolution
Am111	TTL	200ns	0.012mV
μA710	TTL	40ns	1.4mV
Am106	TTL	40ns	0.06mV
μA760	TTL	25ns	0.5mV
NE527/529	TTL	25ns	0.5mV
MC1650	ECL	12ns	30mV

Table I: Propagation Delays of Available Monolithic IC Comparators (100mV Input Step, 5mV Overdrive)

DESIGN OBJECTIVES

In order to achieve the ultimate in speed, it is clear that the comparator outputs must be compatible with ECL, even though at present the majority of systems use TTL. Designers striving for the highest possible speed will already be using ECL in the critical circuit areas of their systems to squeeze the last possible nanosecond out of the overall delay. Further, an ECL circuit requires only one-third the gain of an equivalent TTL circuit for the same resolution owing to its smaller output logic swing. This means that lower impedances can be used and consequently larger bandwidth realized for the same power dissipation. Also, there is no problem interfacing the linear input stages with the digital output gate since an ECL gate is basically a non-saturating overdriven differential amplifier. Properly driving a TTL gate from a linear amplifier is more difficult, however, because it requires a large voltage swing suitably biased to track the input logic threshold with temperature, plus a large peak negative current capability to turn off the gate with minimum delay.

The usefulness and versatility of a comparator can be enhanced by adding a strobe or latch function to the circuit. A strobe simply forces the output of the comparator to one fixed state, independent of input signal conditions, whereas a latch locks the output in the logical state it was in at the instant the latch was enabled. The latch can thus perform a sample and hold function, allowing short input signals to be detected and held for further processing. If the latch is designed to operate directly upon the input stage—so the signal does not suffer any additional delays through the comparator—signals only a few nanoseconds wide can be acquired and held. A latch, therefore, provides a more useful function than a strobe for very high-speed processing.

The most difficult input signal for a comparator to respond to is a large amplitude pulse that just barely exceeds the input threshold. This forces the input stage of the comparator to swing from a full off (or on) state to a point somewhere near the center of its linear range. This exercises both the large-and small-signal responses of the stage. If the comparator has less than 10ns delay under these stringent conditions, then it should be as fast or faster for any other circumstances (see Figure 1). The industry standard measurement is with a

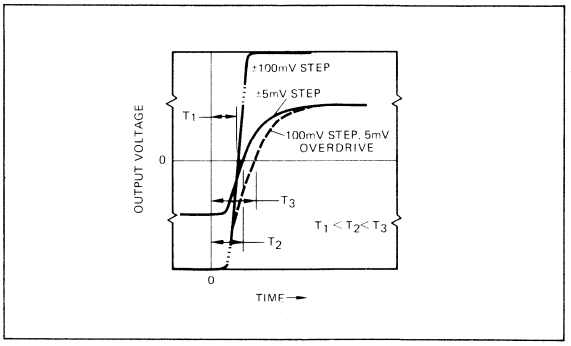


Figure 1. Response to step input signals at output of a differential amplifier

100mV input pulse and an overdrive 5mV above input threshold (this was used for the delays given in Table 1). Pulses larger than 100mV might be used, but this would multiply measurement difficulties, since only a few tenths of a percent aberration or ripple in the pulse generator waveform would be enough to seriously affect the accuracy of the small overdrive, and thus would give misleading results for the propagation delay.

To obtain satisfactory speed for all input signals and particularly for the worst case measurement conditions, the input stage of the comparator must have: 1) wide small-signal bandwidth, 2) high slew rate for large signals, 3) minimum voltage swings, and 4) high gain. The first requirement can be realized by using low-value load resistors, by making every effort in circuit design, device geometry and processing to minimize parasitic capacitances, and by using transistors with the highest f_T possible. The second item calls for high operating currents as well as minimum capacitance. The last two requirements are conflicting, since obtaining high gain normally requires a large voltage swing; therefore some means of clamping the swing must be used that does not degrade the propagation delay.

The overall gain of the complete comparator must also be high because, as illustrated in Figure 1, the propagation delay is less if each stage is well overdriven. To ensure that most of the input overdrive signal is actually used for overdriving, and not consumed in just moving the output from one state to the other, the gain error should be no more than about 10% of the input overdrive. Therefore, for a 5mV overdrive and an ECL output swing of 800mV, the minimum gain must be 1600. It is not practical to strive for much higher gain than this because the small-signal rise time begins to suffer as the stage gain increases. Addition of another stage is undesirable as this also adds delay and increases circuit complexity. It must be remembered that there is a maximum limit on power dissipation that a single integrated circuit package can handle adequately, and this consideration must influence the choice of operating currents and impedance levels throughout the design of the circuit.

With a figure for the total gain required, it is now possible to determine the number of stages and the gain per stage. Since the output stage must be ECL-compatible, its design is fixed, giving a differential-input to single-ended-output gain of about 6. This leaves a differential gain of 270 to be provided by the remainder of the comparator. This is most efficiently divided between two stages, each with a gain somewhat over 16. Both stages should be identical, since minimum overall delay time is obtained when identical stages are cascaded.

A factor not yet discussed that affects the accuracy of the comparator is its input offset voltage. Unless this is trimmed out initially, it must be added to the overdrive in determining the worse-case value of input signal for which the propagation delay specifications will be met. Even with trimming, the temperature drift of high-offset units is typically much greater than that of low-offset units. Therefore, it is desirable to have low initial offset so that trimming is not necessary, and so that the offset temperature coefficient will be good. Also affecting the offset voltage and its drift at higher source resistances are the input currents. To keep this contribution to the total offset low requires high current gains in the input transistors. Therefore, obtaining offsets in the 1–2mV range requires close attention to circuit design, mask layout, and very tight process control (equivalent to that needed for the high-performance, low-frequency operational amplifiers), but with the added kicker of f_Ts well above 1GHz.

As was mentioned, large common-mode and differential voltage ranges are desirable features of a comparator. The limits of the common-mode range in a well-designed circuit should be close to the supply voltages. Since a high-speed comparator will, of necessity, operate at fairly high current levels, the supply voltages must be low to stay within the package power dissipation limits. As a minimum, the common-mode range should be equal to or exceed the differential voltage range to take full advantage of the voltage breakdown characteristics of the input transistors. The basic differential amplifier input stage has a differential voltage breakdown in the range of 5 to 6 volts; the design goal for the common mode range should thus be at least ±3 volts.

In summary, the design objectives for a high-speed precision comparator are as follows:

1) propagation delay <10ns measured at 100mV input step, 5 mV overdrive
2) ECL-compatible outputs
3) latch capability
4) gain >1600
5) input offset voltage <±2mV
6) common -mode range >±3V

CIRCUIT DESIGN

The watchword in designing wideband circuits is simplicity – have the fewest possible active devices in the signal path, the lowest possible impedance levels, and the lowest possible capacitance. The simple, common-emitter differential amplifier can be designed to approach these ideals with one major exception: the deleterious shunting effect of the collector-to-base capacitance upon the driving source resistance is multiplied by the voltage gain of the stage (Miller effect). Even though the impedance levels will be only a few hundred ohms at most, this condition cannot be tolerated if maximum speed is to be achieved. The solution is to add an additional pair of common-base transistors to form a differential cascode amplifier (Figure 2). This circuit has all of the performance features of a common-emitter amplifier and no feedback capacitance.

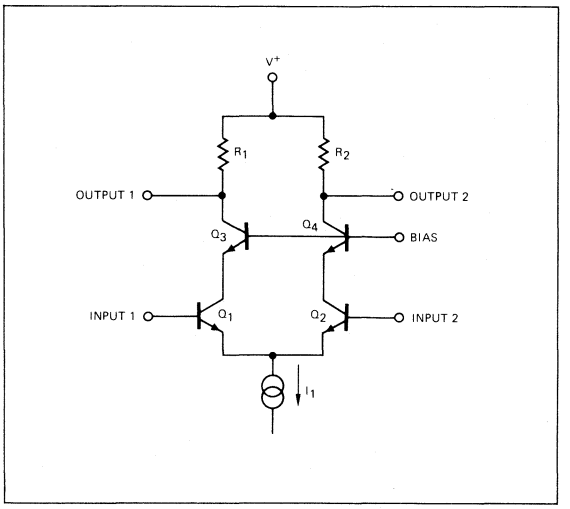


Figure 2. Differential cascode amplifier

Further advantages of the cascode will become apparent later when the latch design is discussed. The only drawback is that there are more devices in the signal path, the positive common-mode range is reduced, and circuitry has to be provided to bias the cascode transistors.

It is now necessary to provide a means of shifting the signal at the output of the cascode (which is very near the positive supply voltage) down to a lower voltage to drive the inputs of the second stage. The use of PNPs is definitely out because of their poor frequency response. This leaves three possibilities: a chain of forward-biased diodes, a programmed voltage drop across a resistor, or a zener diode. The diode chain is useful for level shifts of only a few volts at most, above that, the number of diodes gets too large, with a consequent increase in shunt capacitance and temperature coefficient. The use of a current-source/resistor combination is in the wrong direction for keeping impedance levels low. The resistors could be bypassed with capacitors, but this would offer only marginal improvement, since integrated capacitors have a large shunt component to the substrate. Besides, the addition of four capacitors (for both stages) would result in a large increase in chip area.

The zener diode is definitely superior for high-frequency applications because its shunt capacitance to ground is low, being equal to the collector-to-base capacitance of a transistor. It has no capacitance to the substrate, and its dynamic resistance is quite low. It does have the disadvantage that the level shift is limited to one voltage (6V), which restricts the range of power supply variation the circuit can tolerate. In addition it requires very tight control of the manufacturing process to maintain the matching required. For an input stage gain of 16 the zener voltages have to be matched to better than 0.25% to produce less than 1mV offset voltage at the input.

As shown in Figure 3, the zeners are buffered from the cascode collectors by emitter followers. The pulldown current through the zener-follower combination must be made large enough to discharge the node capacitance when the follower swings in the negative direction. The minimum value necessary is determined by the node capacitance, the signal swing, and the amount of delay that can be tolerated. The amount of signal swing can be reduced by adding clamping diodes across the collectors of the cascode. Regular diode-connected transistors could be used, but would add considerable collector-to-substrate capacitance across the load resistors as well as base-to-emitter capacitance between them. Schottky diodes, on the other hand, require little additional chip area, and are very fast. With clamping, some of the common-mode range lost when the cascode was added can be regained because the cascode transistors can be biased closer to the positive supply without fear of going into saturation at the extremes of the signal swing. The use of Schottky diodes, however, puts a few more gray hairs on the head of the process engineer since he has to control another set of characteristics without affecting the other parameters. The circuit values given in Figure 3 are designed for a minimum differential gain of 16, and a minimum negative-going slew rate at the output of the level-shifter of 1000V/μs.

As mentioned earlier the design of the output stage (Figure 4) can vary little from that of a standard ECL gate. The output emitter followers have to be large enough to handle loading by a 50Ω transmission line (25mA), yet small enough not to add a lot of capacitance that would slow down the response. Therefore, the transistor design must be as efficient as possible with regard to physical size and current-carrying

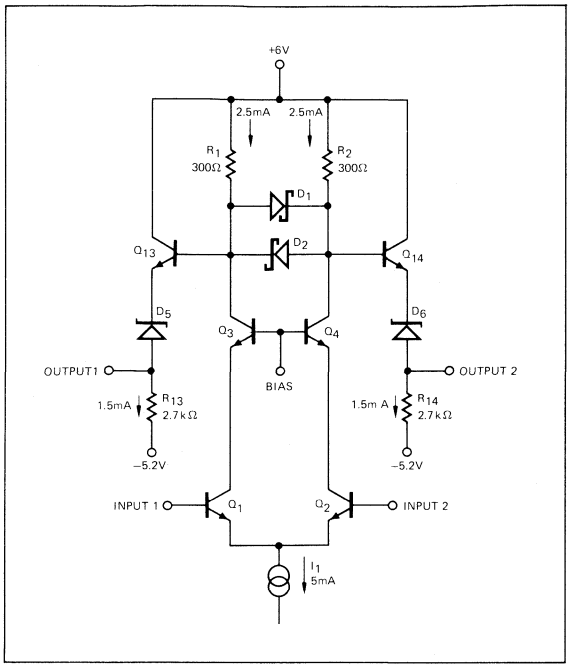


Figure 3. Basic cascode gain stage

capacity. Since the input common-mode level to the gate varies with changes in the power supplies and resistor tolerance, a current source is used to supply the emitters of the gate, rather than the usual resistor to the negative supply. The design of this current source must be such as to provide the correct logical "1" and "0" levels at the output and the proper variation with temperature and power supply changes. The propagation delays to either output of this gate will be equal, whereas they are slightly different in a standard ECL gate owing to the additional capacitive loading on the $\overline{Q}$ output caused by the multiple input transistors.

Implementation of the latch function must be accomplished without interfering with the normal comparator operation or degrading the speed in any way. It must be as close to the input as possible to permit short input signals to be acquired and held. One simple method of adding a latch to a differential

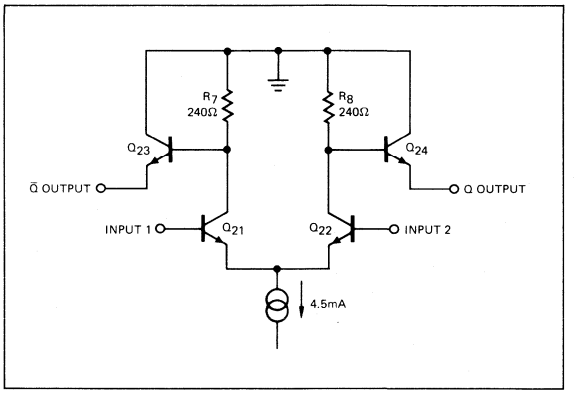


Figure 4. Output gate

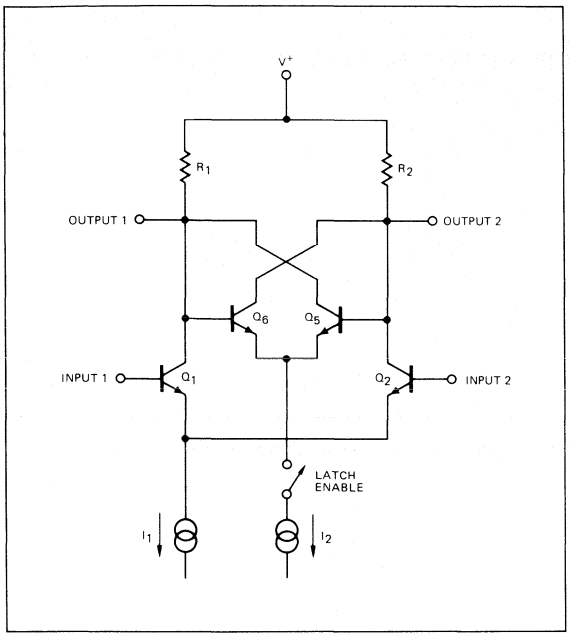


Figure 5. Simple latch circuit

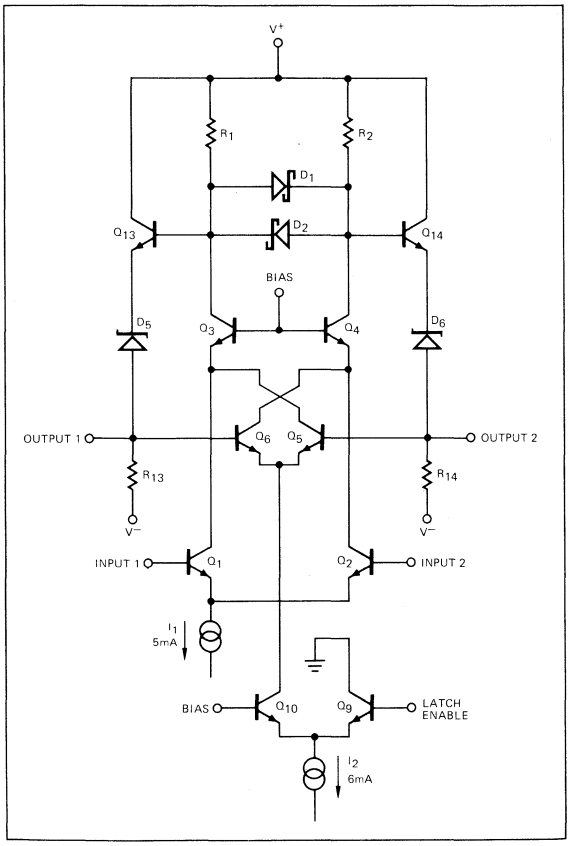


Figure 6. Cascode with latch

amplifier is shown in Figure 5. A pair of transistors, Q_5 and Q_6, are cross-coupled at the collectors of the input transistors, Q_1 and Q_2. The current source I_2 is switched on when it is desired to enable the latch. If I_2 is greater than I_1, the positive feedback via Q_5 and Q_6 will hold the circuit in whatever state it was in when the latch was turned on.

The simple circuit of Figure 5 is not the best for speed because of the added capacitance of Q_5 and Q_6 and the fact that they can saturate unless the signal swings are very small. However, it can be adapted to the cascode stage quite nicely as illustrated in Figure 6. Drive for the positive feedback transistors is taken from the level shifters, and the collectors go to the emitters of the cascode. With this arrangement there is no significant capacitive loading on the gain stage at all. The current source is switched by another differential amplifier, Q_9–Q_{10}, referenced to the ECL logic threshold voltage. This provides the correct input levels for the Latch Enable being driven from a standard ECL gate as well as being very fast, since only currents are being switched.

The latch current source (I_2) must be about 1mA greater than the input current source (I_1) to ensure positive latching for any condition of input signal. Thus, for 5mA in the input stage, at least 6mA must be used to power the latch. This amounts to a lot of power consumed for a function that some users may never even need. However, there is a way to cut the latch standby power down to zero; this is accomplished by the addition of Q_7 and Q_8, as shown in Figure 8.

To understand the function of these transistors, first refer to Figure 7. The differential voltage appearing across the emitters of the cascode transistors is equal to the input signal (for small input signals). This is because the currents through the lower pair of transistors in the cascode are equal to the corresponding currents through the upper pair, and the transistors are matched; therefore the differences in base-emitter voltages must be equal. Thus, Q_7 and Q_8 function as if they were

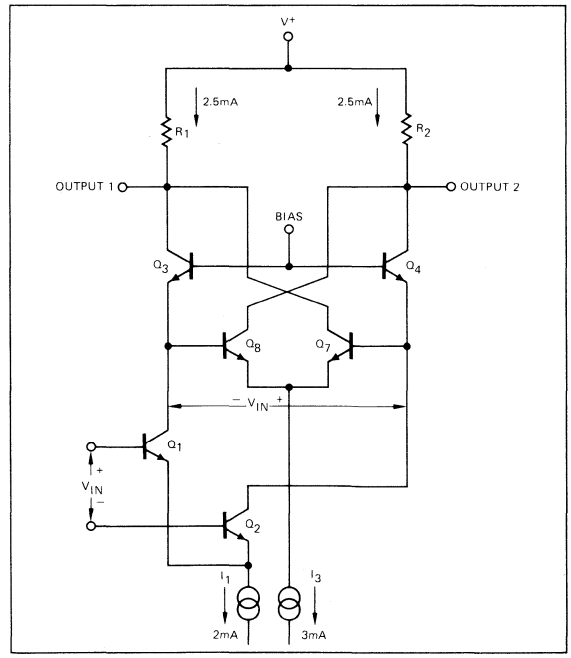


Figure 7. Cascode with "parallel" transistors

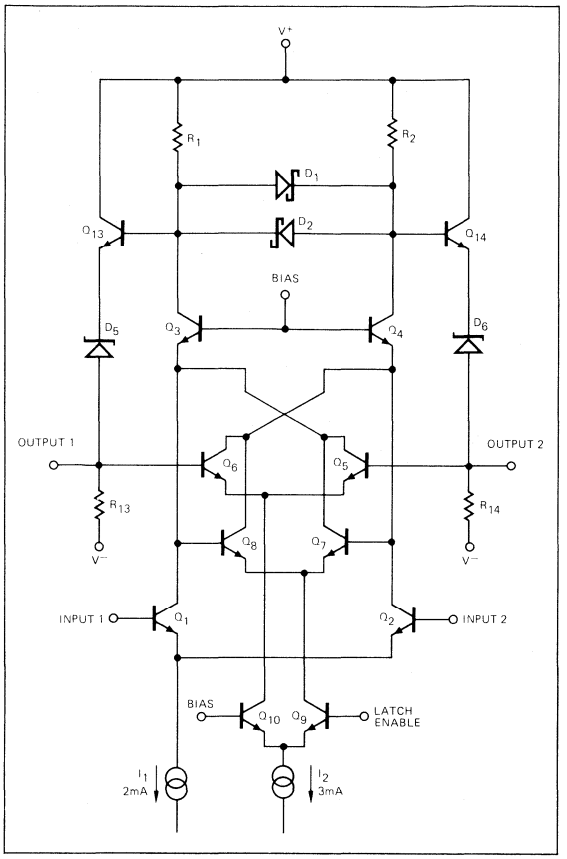


Figure 8. Complete input cascode stage with latch

simply connected in parallel with Q_1 and Q_2, as far as the net effect at the collector load resistors is concerned. To obtain the desired total stage gain, the current I_1 can be 2mA and I_3 can be 3mA.

Now refer to Figure 8. With the latch enable HIGH, Q_9 will be switched on and the 3mA current source will be supplied to the parallel transistors, Q_7–Q_8. The comparator functions normally, and no current is used up in the latch. When the latch enable goes LOW, I_2 will be switched through Q_{10} to the positive feedback transistors, robbing 3mA from the gain stage and giving it to the latch. The latch current is now 1mA greater than the input stage current, but the total current required is still only 5mA. As with the latch transistors, the collectors of the parallel transistors are connected to the emitters of the cascode, so no additional capacitance is added across the load resistors. This places the requirement on Q_7 and Q_8 that they maintain their high f_T at zero collector-to-base voltage.

The use of the parallel transistors has the added bonus that the input bias currents are decreased by more than a factor of two, thus reducing their influence on the offset voltage. The penalty paid is that all three pairs of junctions (Q_1–Q_2, Q_3–Q_4 and Q_7–Q_8) add equally to the input offset. Once again, the processing must be carefully controlled to keep the overall offset within the 2mV goal.

The complete circuit of the comparator is given in Figure 9. It includes some additional refinements as well as the DC biasing. The drive for the latching transistors is taken from the emitters of the second cascode rather than from the level-shifting zeners. This removes their input capacitance from the level shifter and also ensures that Q_{10} cannot saturate. A resistor (R_9) is included to center the common-mode voltage at the input to the gate within its dynamic range; this prevents saturation of the gate or its current source over the expected range of signal swing, temperature drift and supply voltage variations. A separate ground is used for the output emitter followers so that heavy loading at the output will not couple back into the remainder of the circuit. The DC bias chain for the current sources is referenced to ground and the negative supply, so the output logic levels will track those of other ECL circuits connected to the same negative supply. The current sources are designed to stay constant with temperature, which keeps the open-loop gain high at elevated temperatures (>1000 at +125°C), and thus helps to maintain good propagation delay.

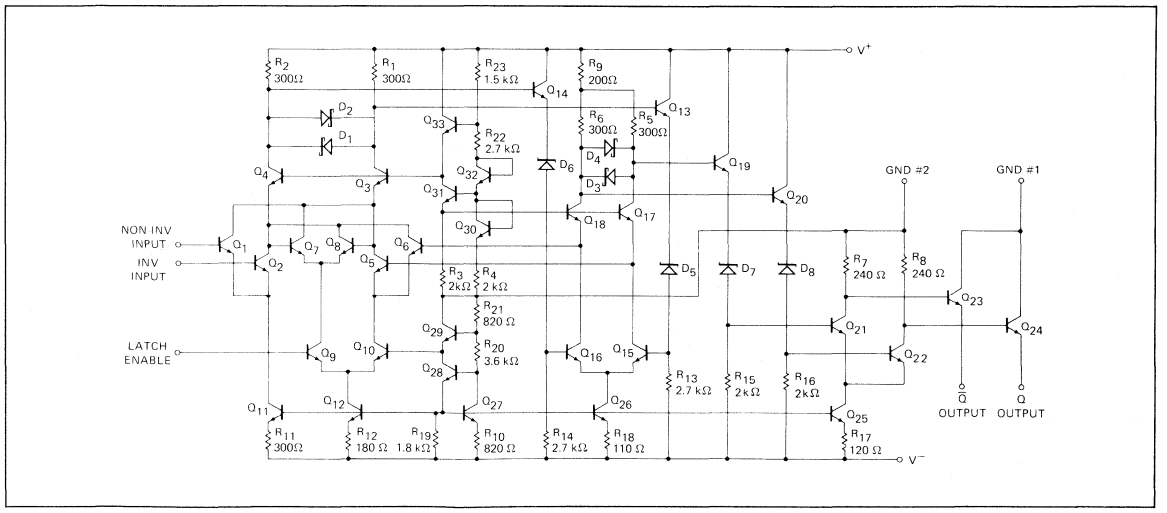


Figure 9. Complete schematic of the Am685 comparator

PROCESS TECHNOLOGY

Circuit design requirements for high speed and a latch function result in an input structure that has three pairs of transistors, the matching of which determines the offset voltage. This dictates that the matching of V_{BE} shall be extremely good between the transistors in each pair in order to meet the 2mV maximum offset voltage target. For the speeds necessary the transistor f_T has to be in the region above 1 GHz, so high-frequency performance can not be compromised. The slew rate of the input stage has to be very high for acceptable response with large input signals. This is achieved by high operating current and low stray capacitances. It is very desirable to keep both the input bias current and the input offset current very low so that the impedances in the source voltages do not introduce intolerable input voltage errors. It would be possible to use a Darlington-connected input stage to achieve these low currents, but the penalty exacted in offset voltage, offset voltage drift, and propagation delay is unacceptable, so high current-gain transistors that match extremely well are needed. The problems are thus centered on achieving very well-matched transistors with high beta and high f_T.

As previously mentioned, it is desirable in a comparator to have a wide common-mode voltage range and high power-supply rejection ratio. This is facilitated by using Schottky diodes to clamp the collector-to-collector swings in the first two stages. Schottky diodes can be fabricated simply by making a window in the oxide over the N-type epitaxial layer and using the same evaporated aluminum as is used for the interconnects (see Figure 10). The contact potential between silicon and aluminum causes a potential barrier to the flow of electrons. Making the metal positive lowers this barrier, allowing electrons to pass over it by virtue of their thermal energy. This process is essentially the same as thermionic emission. Since these electrons are majority carriers, Schottky diodes show extremely fast turn-off characteristics, desirable in this application. Why the Schottky diode is so attractive is that the forward voltage necessary to produce a given current may be several hundred millivolts less than that required to produce the same current in a p-n junction diode of about the same size. It can thus be used as a "clamp" to prevent a bipolar transistor from saturating, when connected from collector to base so as to prevent the forward voltage of the collector-base diode from rising to a level sufficient to cause appreciable current flow in the collector-base diode. This is the common application in Schottky TTL circuits.

In the ECL comparator the use is different. Here they are used back-to-back to limit the differential voltage swings between the collectors in both the first and the second stages. Connected in this way the reverse voltage seen by one Schottky diode is equal to the forward voltage drop of the other diode. Because this voltage is so small reverse leakage is not a great problem. In the simple Schottky diode structure, as described above, the reverse leakage is high. Most of this leakage current is generated at the perimeter of the metal, where there is an electric field concentration. In order to reduce this field the metal is extended all around the opening in the oxide, overlaying this oxide. Spacing the metal from the silicon in this way reduces the field and hence the leakage. In applications where low leakage is critical, the use of a P+ guard ring is called for, but this carries with it extra capacitance, so in view of the fact that the reverse voltage is so low the guard ring technique was discarded for this application. Even so, the diodes used in the comparator have low leakage characteristics with a breakdown at about 45V.

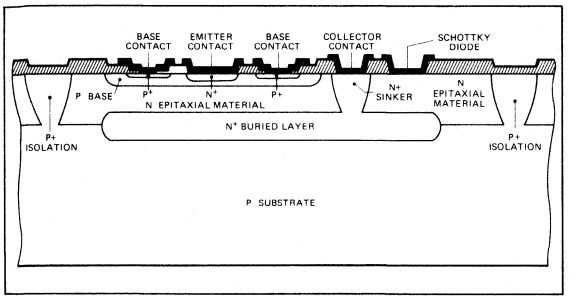


Figure 10. Cross section of transistor and Schottky diode showing sinker and P+ base contact enhancement

At the very high speeds being considered, much effort has to go into reducing capacitances and resistances. Thinning down the epitaxial layer to the minimum required to sustain the voltages encountered is of benefit in two ways: 1) the collector-isolation sidewall area is reduced, lowering the collector-to-substrate capacitance; 2) the collector-series resistance is reduced. The two major contributions to collector-series resistance are the resistance of the epitaxial material between the emitter and the buried N+ layer, and the resistance of the epitaxial layer between the collector contact and the buried layer. However, the first resistance is subject to reduction by conductivity modulation during operation of the device and thus is less important than the second term. The second term can be made very small by using a "sinker", which is a high concentration N-type diffusion from the surface, through the epitaxial layer, to the buried N+ layer. Contact to the collector is then made to the surface of the sinker. (see Figure 10)

Collector-to-base capacitance is held low by using very small dimensions and by using a relatively high epitaxial layer resistivity. The latter also serves to reduce the collector-to-substrate capacitance. A further reduction in collector-to-base capacitance results from using a shallow, high sheet-resistivity diffusion for the base. However, this raises the base resistance, both because the bulk resistance from the contact to the active base region is increased and because the specific contact resistance is increased. These resistances may be reduced by depositing P+ regions under the base contact areas after the main base diffusion.

A compromise has to be made in selecting emitter width. Large emitters are desirable for V_{BE} matching, but very small emitters are essential for high f_T. A stripe emitter, .25-mil wide and 1-mil long, was chosen as optimum. A difference in width, between two otherwise identical emitters, of .01-mil will be sufficient to cause an offset voltage of 1 mV. From this, it can be seen that the photolithography must be extremely carefully controlled, since the offset voltages of three pairs of transistors are summed to give the total offset of the comparator. Because the emitters are so narrow the normal procedure of making a contact cut inside of the emitter cannot be used. Instead, the emitter oxide is simply dissolved in hydrofluoric acid immediately before the aluminum evaporation in order to expose the emitter. As a consequence, the lateral distance between the metal and the emitter-base junction is very small, being equal to the lateral diffusion of the emitter. This means that the sintering process must be carried out at a temperature lower than is customary in linear circuit manufacture in order to avoid short-circuiting the

emitter-base junction by lateral migration of aluminum. An additional reason for lowering the sintering temperature is to avoid penetration of aluminum down through the emitter and base, causing emitter-to-collector shorts.

The requirement for high current gain, for low input bias currents, necessitates narrow base widths. Emitter-to-collector shorts can be a problem in these shallow, narrow-base structures. The probability of shorting can be minimized by careful cleaning procedures and by proper emitter doping levels. Keeping the emitter doping level low also reduces the magnitude of the "emitter dip" effect, whereby the diffusion coefficient of the boron in the region under the emitter is greatly increased by the lattice strain caused by the emitter, resulting in the running-on of the base under the emitter, making it very difficult to achieve a narrow base width.

An area that is neglected in digital circuit processing, because high beta is not necessary, but which is of major importance in linear processing, is the control of surface conditions. If high current gains are to be realized, both the surface area of the emitter-base-depletion region and the surface recombination velocity must be minimized. The former implies that ionic contamination, such as sodium ions, must be eliminated and that the surface state charge density, Qss, should be made as low as possible. The surface recombination velocity is proportional to the fast surface state density and so can be minimized by making this density very low. These three goals; low ionic contamination, low Qss and low fast surface state density are achieved by using the well known techniques of MOS and linear circuit processing, such as annealing in an inert atmosphere and proper choice of sintering cycle.

In the interests of minimum capacitance, the metal interconnects are designed to be narrower than is usual in linear circuits. Special etching techniques have to be employed in order to reproduce these narrow lines reliably. These lines can be seen in the photomicrograph of Figure 11.

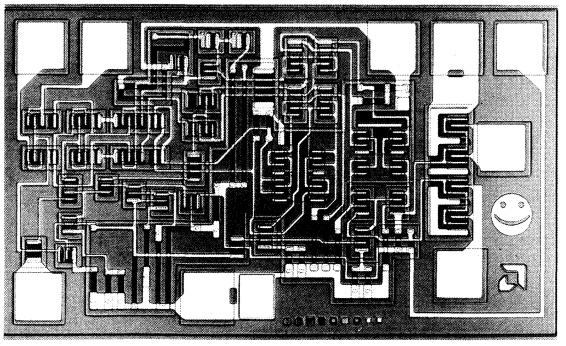


Figure 11. Photomicrograph of the Am685 comparator

PERFORMANCE

The primary design objective for the comparator was to obtain under 10ns propagation delay for large input signals with small overdrive. It should then be as fast or faster for any other input conditions. The performance of the Am685 comparator for a 100mV step input at various overdrives is shown in Figures 12 and 13. The propagation delay is measured from the time the input step crosses the input threshold voltage to the time the output crosses the logic threshold voltage. The input threshold voltage (i.e., the offset voltage) was adjusted for the figures so that the delay can be simply measured by

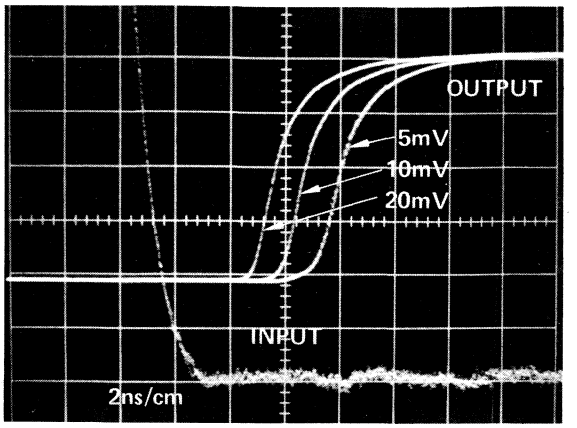


Figure 12. Tpd —"1" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

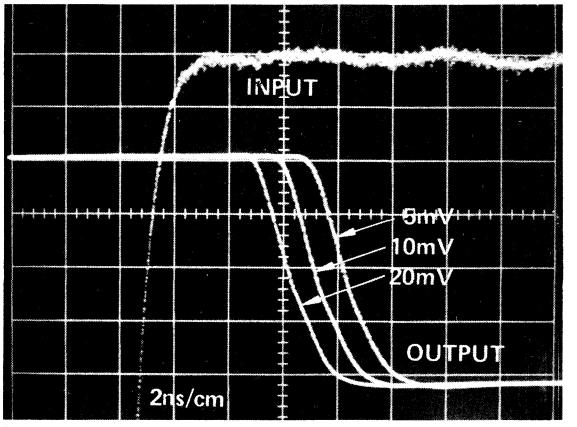


Figure 13. Tpd —"0" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

counting up 5, 10, or 20mV from the bottom of the input pulse. The input pulse, therefore, is displayed on a magnified scale to facilitate this measurement and also to illustrate the purity of input signal required to make accurate measurements at millivolt overdrives.

For a 100mV input step and 5mV overdrive, the propagation delay for a logical "0" is 6.3ns and for a logical "1" is about 300ps less. A graph of delay as a function of overdrive is given in Figure 14. It was previously stated that any other condition

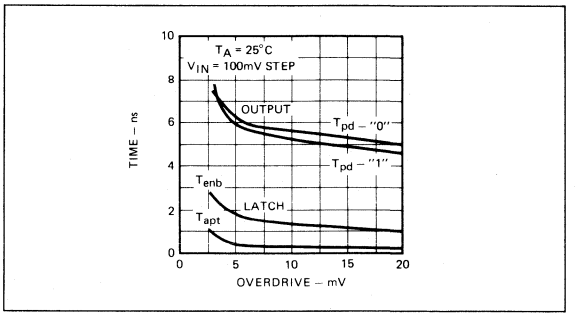


Figure 14. Delay times as a function of input overdrive

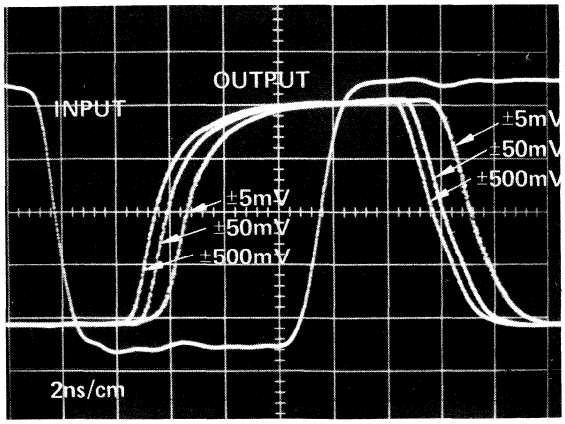


Figure 15. Response to symmetrical input signals

of input signal should give faster response (refer back to Figure 1). This is demonstrated by Figure 15, which illustrates the response of the comparator to symmetrical inputs ranging from ±5mV to ±500mV. The speeds are at least 1 to 2ns faster than for small overdrives.

Figure 16 shows how the delay time varies with temperature. The adverse effects of resistor and gain changes at elevated temperatures result in an increase in delay from 6.3ns at 25°C to 8.4 ns at 85°C and 10.4 ns at 125°C. All of the above data were taken with output loads of 50Ω connected to −2.0V. For lighter loading (such as 500Ω to −5.2V) the output rise and fall times and propagation delays are all slightly faster.

The usefulness of the latch is directly related to how quickly it can be enabled following a change in the input signal. The input signal must be present long enough to pass through the first stage of the comparator before the latching transistors can act upon it. The minimum time that the input must be present before the latch can be turned on is defined as the latch enable time. This is measured as the minimum time that must elapse

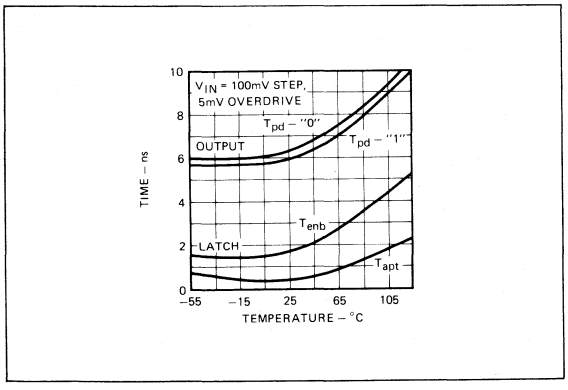


Figure 16. Delay times as a function of temperature

between the time the input step crosses the input threshold voltage and the time the latch enable input crosses the logic threshold voltage for which the comparator outputs will assume the correct states.

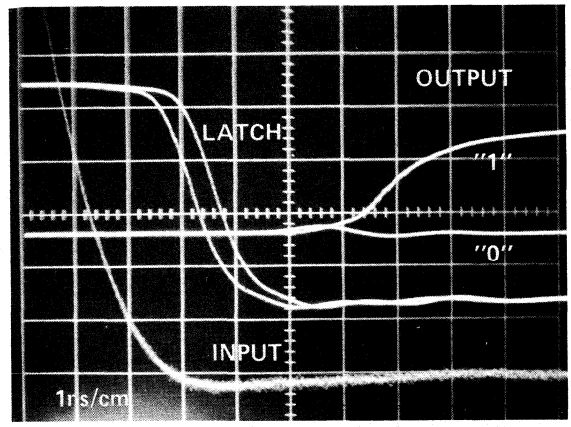


Figure 17. Latch enable time and latch aperature time for 100mV input step, 5mV overdrive (input = 5mV/cm, latch = 200mV/cm, output = 400mV/cm)

The performance of the latch function is illustrated by Figure 17. The input signal is the standard 100mV step with 5mV overdrive and is in the direction to cause the output to switch from a logical "0" to a logical "1". The delay of the latch signal relative to the input is adjusted until the output just switches to a "1"; this is the latch enable time and under these conditions is 1.8 ns. The difference between the latch timing for which the output just barely switches and when it does not switch is the latch aperture time; this is about 500ps for 5mV overdrive. The performance of the latch with input overdrive and temperature generally follows that of the propagation delays (Figure 14 and 16).

The overall performance of the Am685 is summarized in Table II. It is apparent from the table and the previous discussion that the device is ideally suited for applications where both precision and high speed are required, such as in analog-to-digital converters, data acquisition systems, and optical isolators. The device is the first in a family of new wideband linear integrated circuits designed to meet the requirements of very high-speed systems.

Propagation Delay (100mV step, 5mV overdrive)	26.5 ns MAX
Input Offset Voltage	2.0mV MAX
Average Temperature Coefficient Of Input Offset Voltage	10μV/°C MAX
Input Offset Current	1.0μA MAX
Input Bias Current	10μA MAX
Common Mode Voltage Range	±3.3V MIN
Common Mode Rejection Ratio	80dB MIN
Supply Voltage Rejection Ratio	70dB MIN
Positive Supply Current	22 mA MAX
Negative Supply Current	26 mA MAX

Table II: Performance Characteristics of the Am685 Comparator (T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, R_L = 50Ω to −2.0V)

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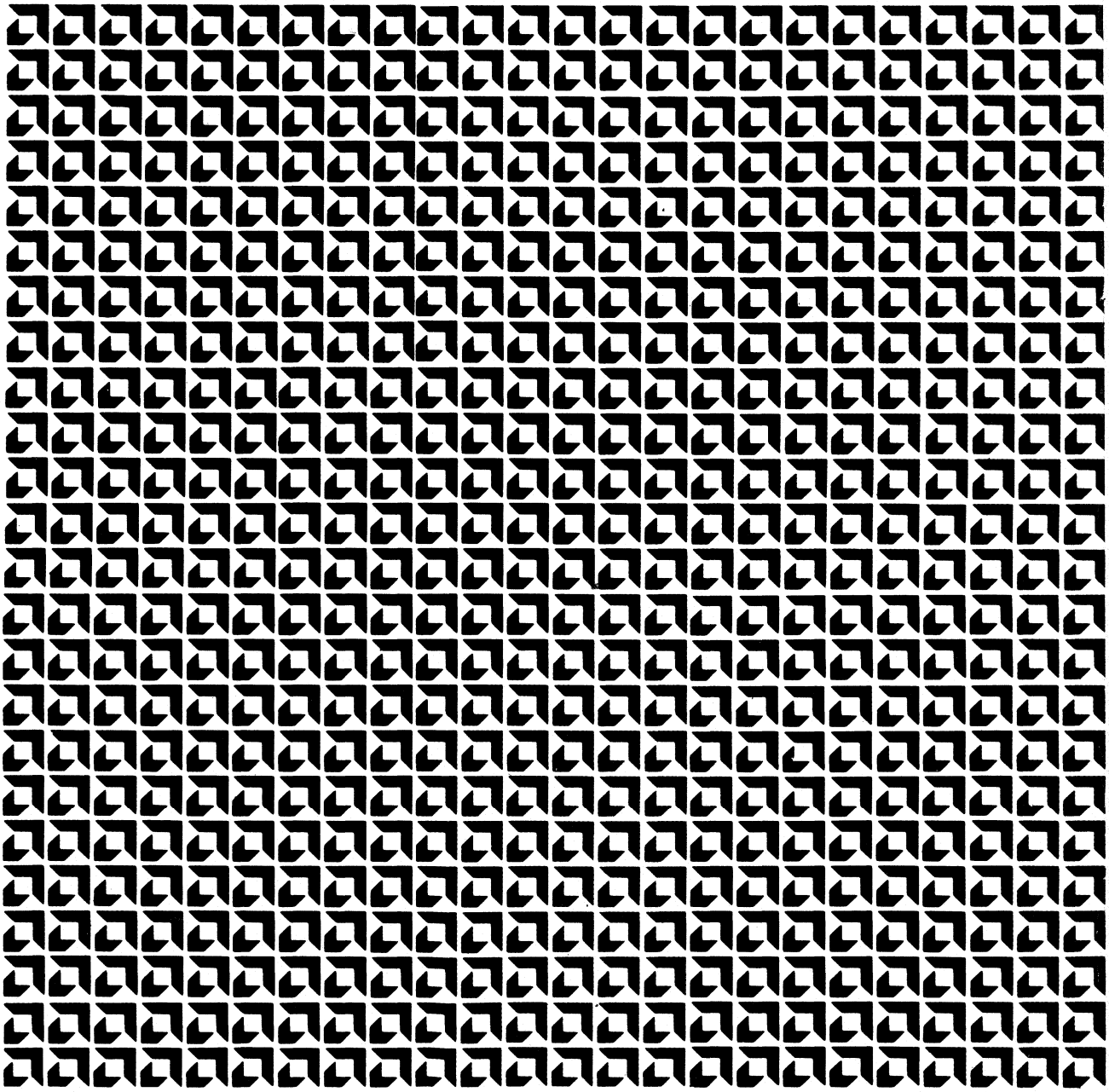

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